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Energy Efficient Branch and Bound based On-Chip Irregular Network Design

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Abstract

Here we present a technique which construct the topology for heterogeneous SoC, (Application Specific NoC) such that total Dynamic communication energy is optimized. The topology is certain to satisfy the constraints of node degree as well the link length. We first layout the topology by finding the shortest path between traffic characteristics with the branch and bound optimization technique. Deadlock is dealt with escape routing using Spanning tree. Investigation outcome show that the proposed design methodology is fast and achieves significant dynamic energy gain.

Index terms— network on chip, shortest path, branch and bound, routing.

1 Introduction

nterconnection networks are used to meet the communication demands of the numerous processing elements in high end parallel supercomputers, telecom switches and more recently their wide spread use is also seen for the communication requirement in complex SoC [1] having numerous processing elements. With the development of integration technology, System on Chip composed of numerous cores on a single chip has entered the billion transistor era. As the microprocessor industry moves from single core to multi core architectures, requiring efficient communication among processor. A high performance, flexible, scalable and design friendly interconnection network design is highly preferred for new SoC and chip designs. These interconnection networks for complex SoC also referred as on chip Networks. Network on chip have emerged as a viable option for scheming scalable messaging architecture for MPSOCs .In Noc, on chip micro networks are used to intersect the various cores, which are better than bus based systems, so used for dealing communication issues. Early works are done for standard topologies like mesh, torus etc where traffic cannot be statically predicted however challenges are different for diverse SoC with different core size, operation and communication requirement. In Irregular NoC each node can be connected to one or more core, as per the constraint and design requirement and therefore are best suited for application specific custom NoC design [2,3]. Here we propose a branch and bound **??**B&B] Author ? ? ?: Deptt. Of CSE, CTAE, MPUAT, Udaipur. e-mails: kalpana_jain2@rediffmail.com, naveenc121@yahoo.com, dharm94@gmail.com based heuristics for the design of customized energy efficient irregular NoC assuming an area optimized floor plan as a prerequisite.

2 II.

3 Communication Energy and

Design of Irregular Network on Chip has two main issues to be dealt with respect to the proposed work that is calculating energy dissipated through the network for data transfer and finding the routes between the cores of network. Thus here we discuss the Energy Model and Routing methods used. a) Energy Model Ye et al. [4] proposed a model for communication for on chip networks. For regular networks the channels length between the

cores is of uniform length. Thus the energy dissipated in transferring 1 bit of data from soured core to destination core comprising of both router energy and channel energy is as follows: Router Energy: (E Rbit) E Rbit = E Sbit + E Bbit + E Wbit (1) Where E Sbit + E Bbit + E Wbit correspond to the dynamic energy elapsed by switch(E Bbit), buffering(E Bbit) and interconnection links (E Wbit) within the switching framework. The dynamic energy dissipated on the channels between cores (E Lbit) should also be considered, thus the dynamic energy dissipated in transferring one bit of information from a tile to its adjacent tile can be given as E bit = E Rbit +E Lbit (2) Thus the communication_energy required in sending 1 bit of information from source tile t j to destination tile tile t k is Where nhops is sum of tiles from source tile tj to destination t k and E Lbit is channel length between adjacent tiles (channel length is uniform for all adjacent tiles of regular networks).

For irregular networks the channel length is not of uniform (equal), as channels are laid by maximum length constraint of link length. Thus the second operand of eq-3 is replaced as the summation of energy dissipated by each channel in the route of source tile t j to destination tile t k The popular routing algorithms with irregular topologies such as Left-Right routing [8], up -down routing [6] etc, uses the turn based model [7] to overcome deadlock state. In the proposed work minimum shortest paths are laid as preferred routing paths from the source tile to destination tile with a view to optimize communication energy requirements, however a methodology based on escape route [5] is used to achieve deadlock freedom in communication.

4 III. Proposed Methodology for Energy

Efficient Branch and Bound based on Chip Irregular Network Design

In the presented work, an energy efficient topology design is proposed. To design the energy efficient topology the, the channels laid should be such that they lead to shortest path for communication, this is achieved by finding the shortest path application communication characteristics, considering the constraints of node degree and length of channel as maximum length should not be exceeded due to physical signaling delay. Moreover the connectivity of network is assured by creating spanning tree for the network and a constraint according to up/down routing, is used to achieve the deadlock freedom in communication. The application characteristics are clustered according to the source traffic, and then using the shortest energy path as the optimization criteria and a branch and bound method is developed to get an customized energy efficient irregular on-chip network then the source with the maximum data rate are routed using shortest path and branch and bound method used to get the optimized solution.

The design flow is given in figure **??** shows the input taken for topology synthesizer such as traffic characteristics, constraints and tile coordinates for Manhattan distance to lay the channel. a) Branch and Bound (B&B) Topology Generation A branch and bound [19] based optimization technique is developed to design a dynamic communication energy efficient methodology, which is custom tailored according to the traffic requirement (predefined) with the necessary constraints of node degree , channel length and routing. Figure 2 shows the partial representation of nodes generation of tree, traffic requirement is routed at each stage to form the efficient communication energy topology.

The nodes of the tree can be one of the following types: UBC and LBC are cost of the nodes which helps us to determine the whether the nodes lead to optimal solution and helps in not making the search exhaustive.

Finding optimal solution for the problem of efficient communication energy topology is searching leaf node with minimum cost. Branch is expansion(create child node) at each node by routing next application characteristics to be routed, and bound is check on child nodes whether they lead to the better solution. This checking is achieved by comparing their UBC and LBC with the global UBC and parent node. If cost or LBC is greater than global_min_UBC child nodes are discarded.

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Volume XIV Issue IV Version I b) The calculation of UBC and LBC UBC calculation: UBC of node is calculated by finding path of all remaining unrouted traffic characteristics using a greedy method for remaining unrouted traffic characteristics.For each step in the greedy method , the next unmapped application characteristics with highest communication demand is selected and its path is laid by shortest path method. This step is repeated until all application are routed. This leads to a complete routing and identifies a leaf node. If this node is illegal then it is discarded otherwise saved for the future expansion.

LBC calculation: LBC of node is calculated by finding path of all remaining unrouted application characteristics, here constraints of topology are not considered in path setup. This step is repeated for all remaining unrouted traffic characteristics.

Priority Queue is used to speed up the search for optimal leaf node; the nodes are inserted in sorted order of their cost, once the Queue is full, nodes are inserted only if they are leading to better solution.

c) The Proposed methodology: Algorithm IV.

6 Experimental Results

The random data sets required to evaluate the proposed methodology was generated using TGFF [18] with diverse communication data rate of the cores. An On Chip simulator is used for evaluation. The router energy dissipated is evaluated using the power simulator Orion [15,20] for 0.18?m technology. The dynamic bit energy

dessipated for inter-node link (ELbit) can be computed using the below equation. E Lbit = (1/2) x ? x C phy x V 2 Where 1. ? = average probability of a one to zero or zero to one transition between two successive samples in the stream for a specific bit, assured average value of ? = 0.5. 2. C phy = physical capacitance of inter-node wire. 3. V DD is the supply voltage.

Below graphs shows the evaluation comparison of proposed methodology with Genetic algorithms based methodology proposed [14] by Naveen Choudhary et al. for the similar data sets (tile coordinates and traffic characteristics) with Node_degree =4 and link length as twice the length of the Maximum core size.

Below Graphs shows the performance comparison of Branch and Bound and [14] over 100 sets of diverse application data. Average flit latency gain in the range of 5% to 20% and average communication energy gain in the range of 2% to 10% in comparison to [14] has achieved by the topologies generated by the proposed B&B method.

7 Conclusion

The paper present a B&B based technique for designing an energy efficient custom tailored topology for Irregular on-chip networks. The customized topology is design as per the predefined traffic requirements. The necessary constraint of max node degree, max channel length, deadlock free communication and area optimized floor plan are incorporated in the proposed methodology provides a realistic solution .The results clearly elaborates that the proposed method is able to generate better energy efficient networks in comparison to the popular evolutionary based approach [14].

The proposed work can be further extended in a quite few ways such as incorporating the floor plan also in the proposed methodology which can be expected to provide improved energy efficient networks may be at the cost of increased area overhead. Another extension of the proposed work can be in the area of designing irregular 3D on-chip energy efficient networks.

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Figure 1: I

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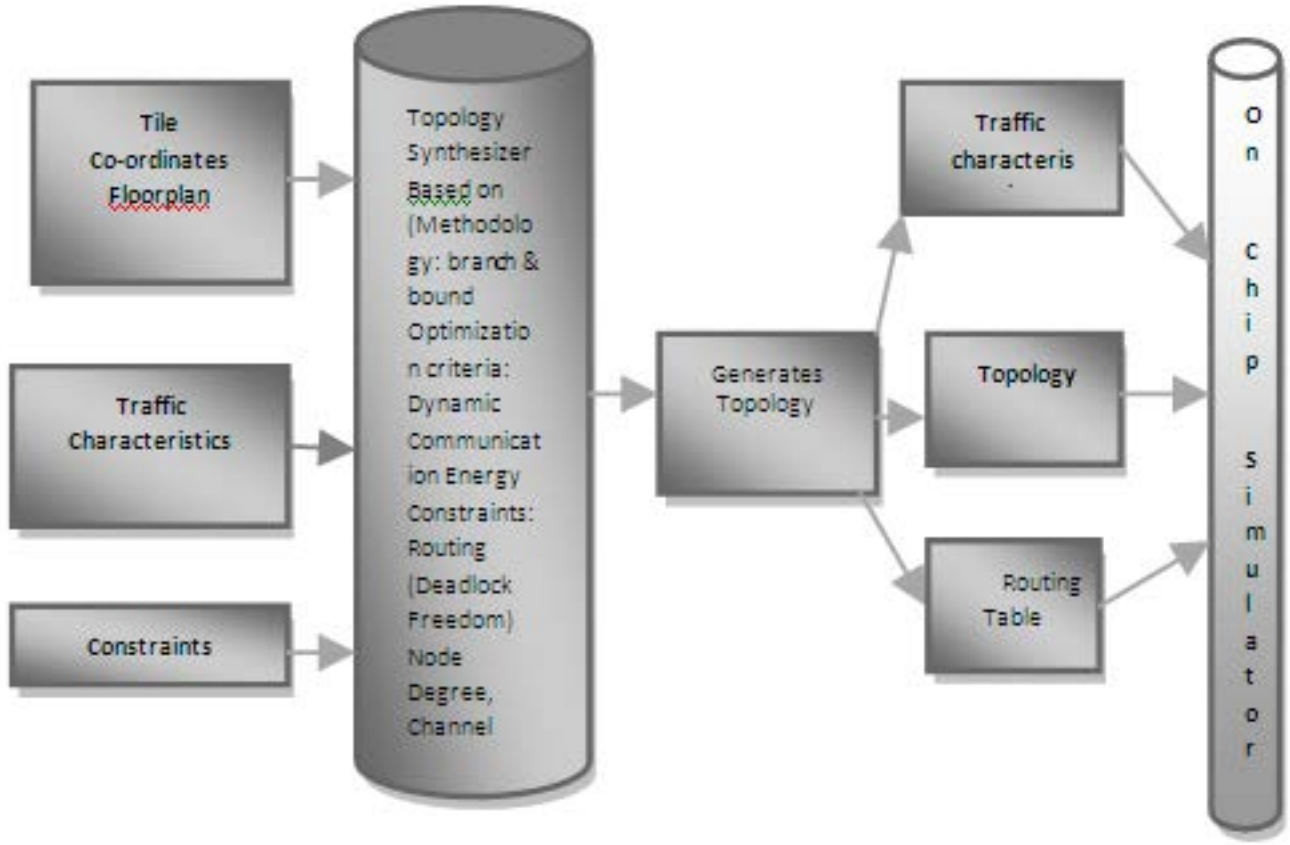
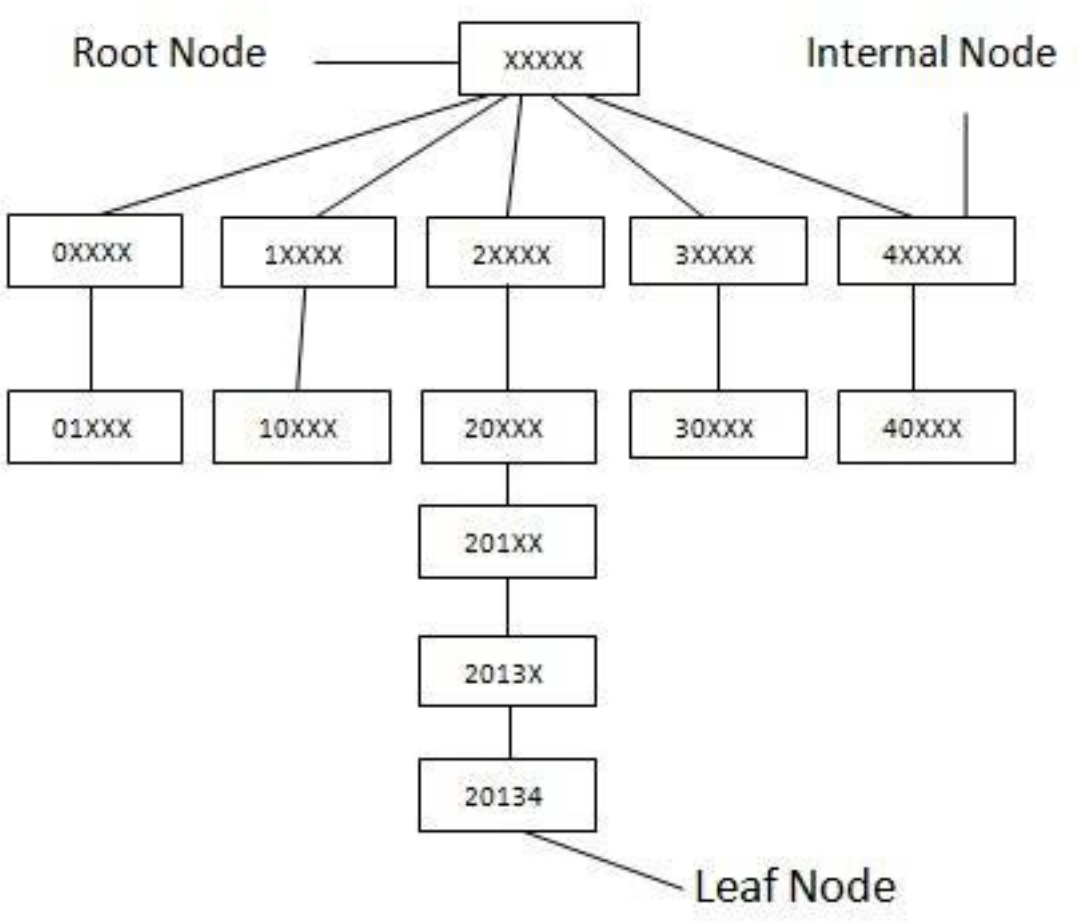


Figure 2: Figure1:


Root Node
XXXXX
Internal Node
0XXXX
1XXXX
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201XX
2013X
20134
Leaf Node

Figure 3:

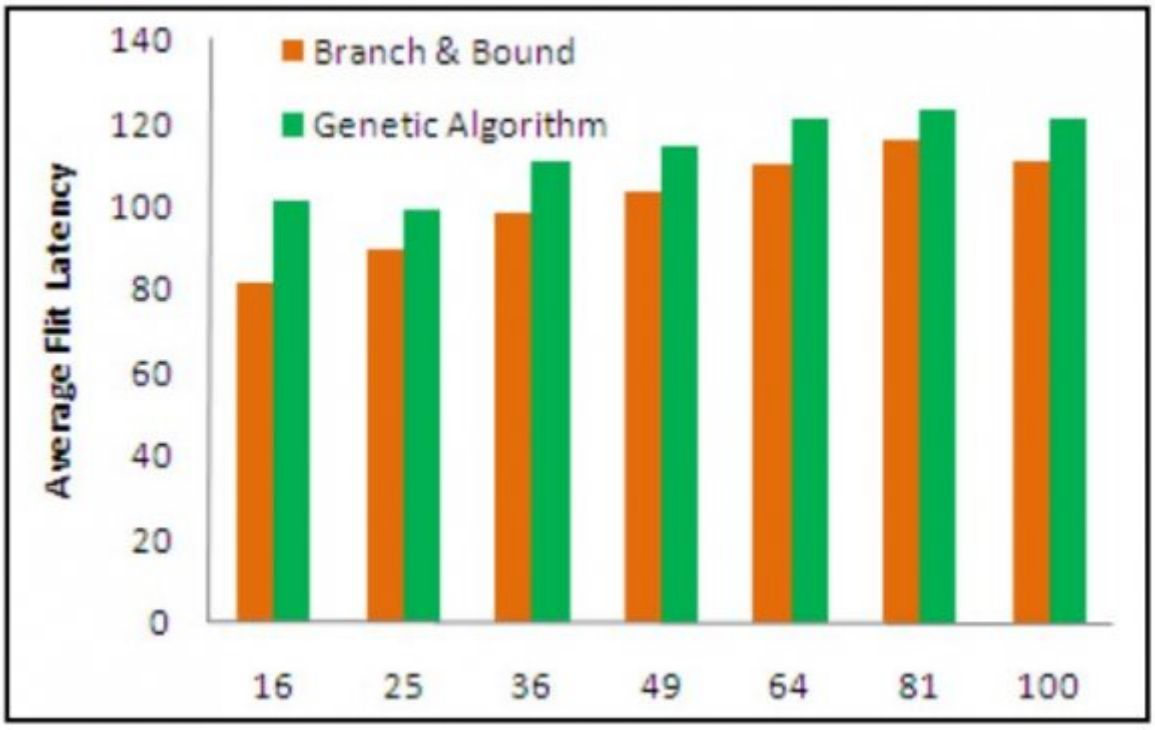

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Figure 4: Figure 2 :

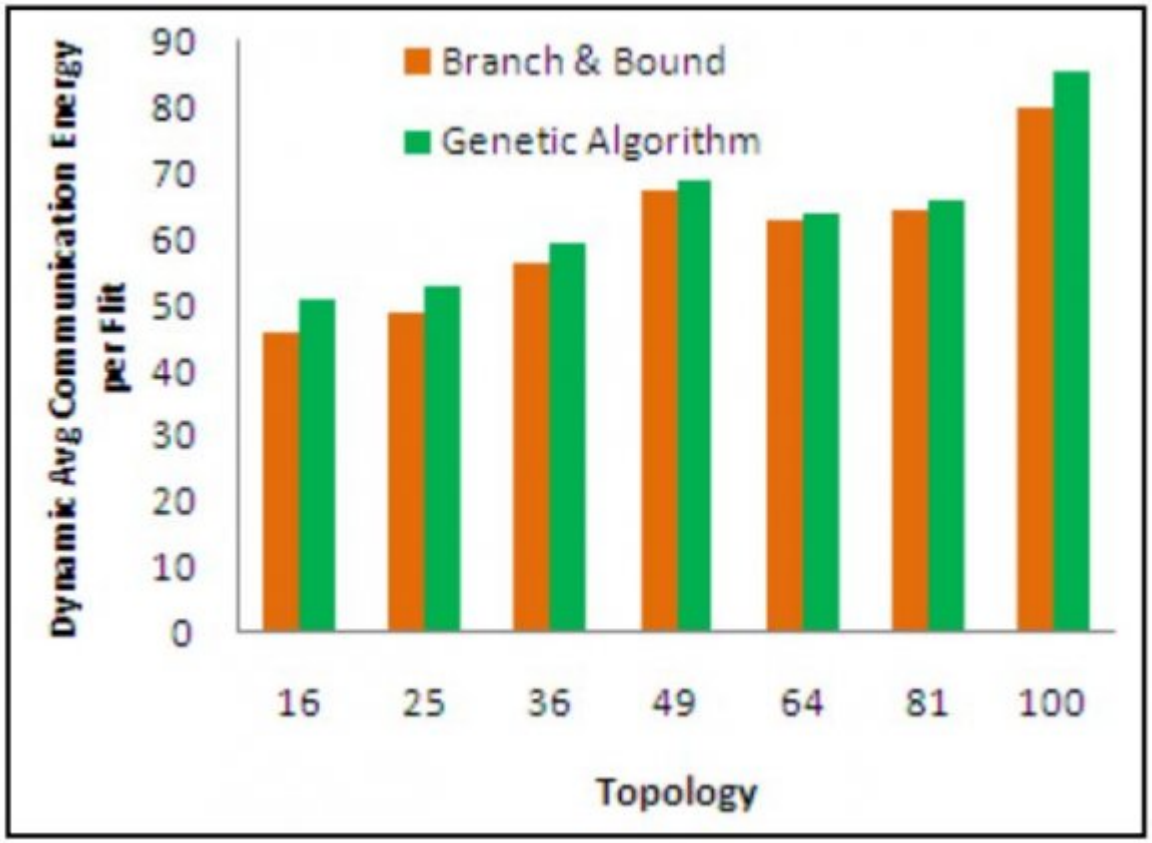
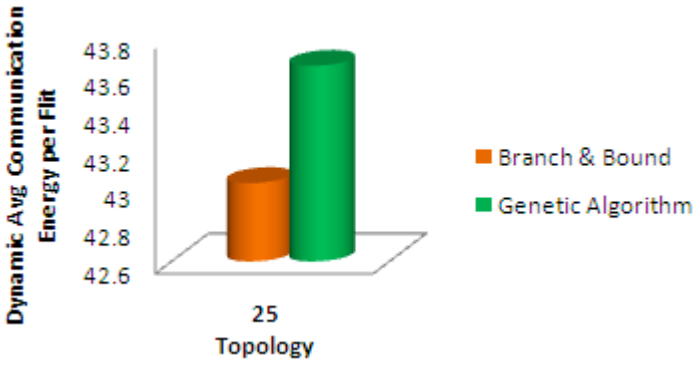


Figure 5:



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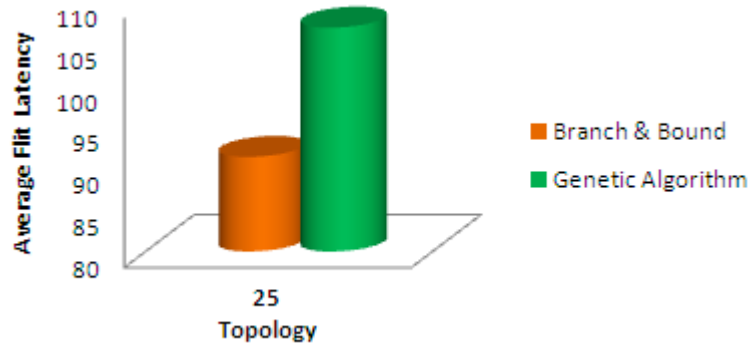

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Figure 7: Figure 3 :Figure 4 :

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