



GLOBAL JOURNAL OF COMPUTER SCIENCE AND TECHNOLOGY: E
NETWORK, WEB & SECURITY

Volume 15 Issue 6 Version 1.0 Year 2015

Type: Double Blind Peer Reviewed International Research Journal

Publisher: Global Journals Inc. (USA)

Online ISSN: 0975-4172 & Print ISSN: 0975-4350

Noc Evolution and Performance Optimization by Addition of Long Range Links: A Survey

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GJCST-E Classification : D.3.4



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Noc Evolution and Performance Optimization by Addition of Long Range Links: A Survey

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1. INTRODUCTION

Present day VLSI technology permits to build systems with millions of transistors on a single chip to meet the growing computational applications and to achieve high performance with low-power/energy requirements. A system on a chip or system on chip (SoC) is an integrated circuit (IC) that integrates all components of a computer or other electronic system into a single chip but the interconnection between each other is a challenging issue [2]. Traditionally, the interconnection networks used for communication among the components in a system on chip were bus-based and point to point links. In a shared bus interconnection network, many masters and slaves share the bus with each other but only one master at a time can use the bus, and the other masters have to wait for their turn so a bus arbiter makes a decision among multiple bus access requests. The shared bus architecture was used because of its low-cost and simple installation characteristics. However, it has limitation in its scalability because only one master at a time can use the bus at a time. It becomes a communication bottleneck when the number of bus requesters grows tremendously and the bandwidth is limited. Dedicated point-to-point links improves latency, power usage and bandwidth availability. But as the number of IPs grows, the number of dedicated point-to-

point interconnections grows exponentially resulting in a larger realization area [3]. A solution that satisfies scalable bandwidth requirement is "Network on Chip (NoC) architecture". Dally and Towles proposed that NoC eliminate ad-hoc global wiring and introduced on-chip interconnection network with modular design which gives better performance, higher bandwidth, and scalability and reusable components. NoCs use packets to route data from the source Processing Element (PE) or node to the destination PE or node via a network fabric that consists of network interfaces, routers and interconnection links [1].

A research on network-on-chip (NoC) depicts a change of state from computation-centric to communication-centric design paradigm by development of scalable communication structures and thus achieving global communication in SoC [4].

A 2D mesh topology is a regular grid-like NoC architecture which has a simpler design layout. They have well-controlled electrical parameters and reduced power consumption on the global wires. Such architectures have long packet latencies although the shortest path algorithms are used because here the packet have to travels many hops to reach to the destination node which leads to an energy inefficient architecture [6].

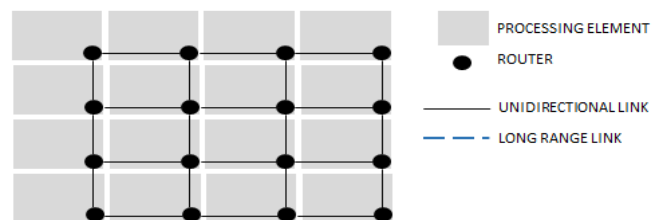


Figure 1 : A standard 4x4 2D mesh network

A completely new concept is proposed of laying few long rang links on the top of a regular 2D mesh network depending on the communication traffic characteristics of various applications to reduce the number of hops between the communicating nodes. Thus, reducing the average latency of a packet and thereby, improving the performance of the entire network [5].

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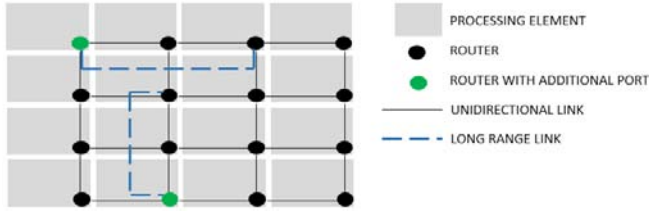


Figure 2 : Long range links are added to a standard 4X4 mesh network

In this survey paper, we summarize the evolution and necessity of NoC. We have shown the NoC architectures for a standard mesh network and also modified the same by addition of long range links. For the convenience in Section II, computations are shown to calculate average packet latency and Manhattan distance for a standard mesh network and for network using long range links. In Section III, turn model is discussed. In Section IV, energy model is shown. Lastly, conclusion followed by the future scope is discussed in section V.

II. COMPUTATIONS

For random traffic patterns categorized by the communication frequencies f_{ij} , τ_0 is computed by the author [5] written as follows:

$$\tau_0 = \sum_{i \neq j} f_{ij} \left[d(i,j)(t_r + t_s + t_w) + \max(t_s + t_w) \left\lceil \frac{L}{W} \right\rceil \right] \quad \text{Eq. 1}$$

where $d(i,j)$ is the distance from routers i to router j , and t_r , t_s , t_w are the is architectural parameters representing time to make the routing decision, traverse the switch and the link, respectively. Finally, L is the length of the packet, while W is the width of the network channel.

For the standard mesh network, the *Manhattan distance* (d_M) is used to compute $d(i, j)$ where x and y denote the x - y coordinates. [5]

$$d_M(i,j) = |i_x - j_x| + |i_y - j_y| \quad \text{Eq. 2}$$

For the routers with long-range links, [5]

$$d(i,j) = \begin{cases} d_M(i,j) & \text{if no long-range link is attached to } i \\ \min(d_M(i,j), 1 + d_M(k,j)) & \text{if } l(i,k) \text{ exists} \end{cases} \quad \text{Eq. 3}$$

In the above equation, $l(i,k)$ means that node i is connected to node k via a long-range link [5].

An example shown below demonstrates that the use of long range link decreases the number of hops traversed by a packet for reaching to the destination node.

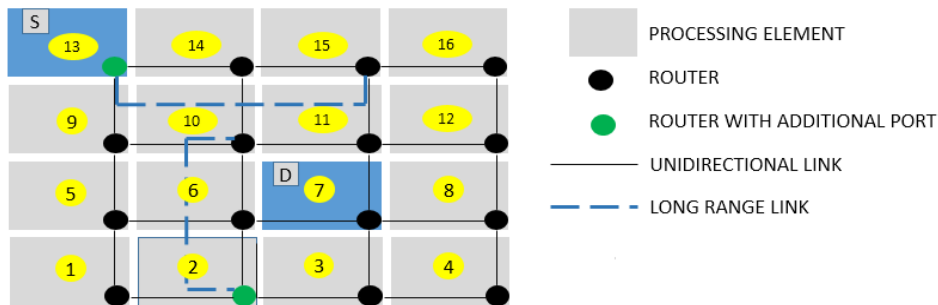


Figure 3 : A standard 4x4 2D mesh network where S and D represents source and destination respectively

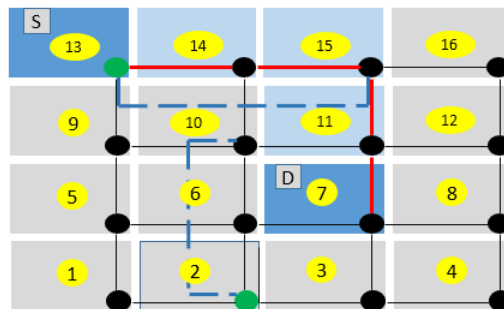


Figure 4 : XY Routing [8] path for reaching from source node to destination node and the nodes visited in between for a standard mesh network

The x,y coordinates for source node, 13 and destination node, 7 are (0,3) and (2,1) respectively. Therefore, $d_m(i,j) = 4$

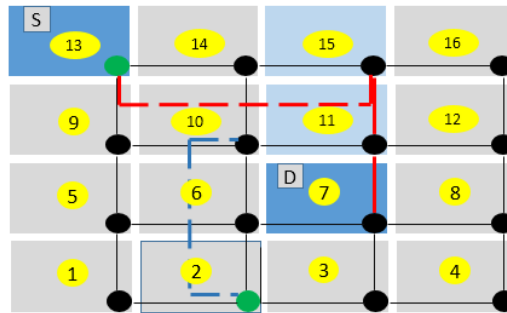


Figure 5 : XY routing path for reaching from source to destination node using long range link.

Now, calculating $dm(i,j)$ for the above figure using long range link,
 $d_m(i,j) = 3$

III. TURN MODEL

A packet traverses through various nodes as it moves from source to destination. At each hop a decision is to be made whether to move straight or take

a turn along a routing path. This decision is significant because a wrong turn may lead to cyclic dependencies which may further cause a deadlock due to which packet is unable to reach destination. Some combinations of turns are proposed which are deadlock free. This is called turn model [10]. A packet has to follow turn model till it reaches to destination.

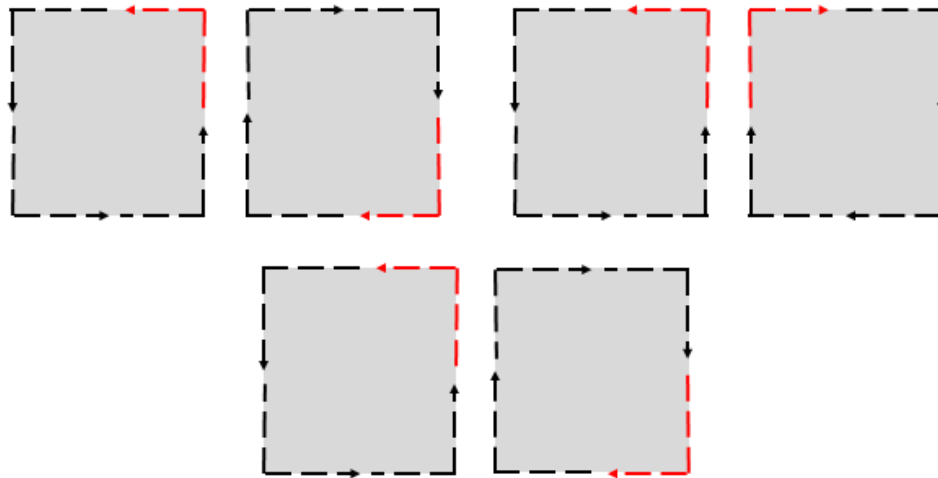


Figure 6 : Turn Model [10]: Turns shown in black are allowed while turns shown in red are prohibited.

IV. DYNAMIC COMMUNICATION ENERGY MODEL

The dynamic communication energy model for the network on chip can be defined as:

$$E_{bit}(t_i, t_j) = n_{hops} \times E_{rbit} + (n_{hops}-1) \times E_{Lbit} \quad \text{Eq. 4}$$

Where $E_{bit}(t_i, t_j)$ is the average energy consumption for sending one bit of data from t_i to tile t_j , n_{hops} is the number of routers the bit traverses from tile t_i to tile t_j , E_{rbit} is the energy consumed by the router for transporting one bit of data and E_{Lbit} is the energy consumed by unit link/channel for transporting one bit of data.

To reduce energy consumption, it is important to identify the energy efficient architectures. Therefore

the energy-performance trade-offs need to be considered. Depending on the parameter selected an efficient methodology is proposed that is to be designed based on the selected performance metrics with help of long range interconnects for standard grid based network [9].

V. CONCLUSION

We have summarized the evolution and necessity of NoC by showing the disadvantages of buses over NoC architectures. We have shown the NoC architectures for a standard mesh network and also modified the same by addition of long range links. By taking an example we have shown that by adding long range links to a mesh network number of hops traversed by a packet. Hence, we found that there is a

significant reduction in the average packet latency and increase in network throughput.

VI. FUTURE SCOPE

For exploring more network structures and to reduce energy consumption and wire delay, we can intend to explore the effect of long rank interconnects/links based on the application specific traffic load for constant bit rate traffic with practical constraints on link length and the port availability per tile. The feasibility of the proposed design is planned to be explored for 2D as well as 3D NoCs. A 3D NoC is the stack of 2D NoC in such a way that each stack is again connected to its front and rear stack. It was proposed that in 3D NoC, the numbers of hops traversed by the flit towards the destination are reduced, thereby, have the following advantages such as high throughput, reduced message latency and energy dissipation as compared to the traditional 2D NoCs [10]. So we propose that the long range links when inserted in a 3D NoC topology will give drastically good results in terms of high network throughput and reduced average packet latency.

REFERENCES RÉFÉRENCES REFERENCIAS

1. W. Dally, B. Towles, "Route packets, not wires: On-chip interconnection networks," In Proc. DAC, June 2001.
2. L. Benini, G. De Micheli. "Networks on chips: A new SoC paradigm," IEEE Computer. 35(1), 2002.
3. Hyung Gyu Lee, N. Chang, Umit Y. Ogras and R. Marculescu, "On-chip communication architecture exploration: A quantitative evaluation of point-to-point, bus, and network-on-chip approaches", ACM Transactions on Design Automation of Electronic Systems, vol.12, no.3, article 23, 2007.
4. T. Bjerregaard and S. Mahadevan "A Survey of Research and Practices of Network-on-Chip" ,ACM Computing Surveys, vol.38., 2006.
5. Umit Y. Ogras and R. Marculescu "Application-Specific Network-on-Chip Architecture Customization via Long-Range Link Insertion", 2005.
6. Umit Y. Ogras and R. Marculescu "It's a Small World After All: NoC Performance Optimization Via Long-Range Link Insertion", IEEE, VOL. 14, NO. 7, July 2006.
7. N. Choudhary Network-on-Chip: A New SoC Communication Infrastructure Paradigm. International Journal of Soft Computing and Engineering (IJSCE), ISSN: 2231-2307, vol.1, 332-335.
8. W. Zhang, L. Hou, J. Wang, S. Geng, W. Wu, "Comparison Research between XY and OddEven Routing Algorithm of a 2-Dimension 3X3 Mesh Topology Network-on-Chip" 2006
9. C. J. Glass and L. M. Ni, "The turn model for adaptive routing," in Proc. ISCA, 1992, pp. 278–287.
10. M. K. Puthal, M. S. Gaur, and V. Laxmi, "Performance Comparison of 2D and 3D Mesh NoC," 2011.