

An Efficient Routing Implementation for Irregular Networks

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Abstract

with the recent advancements in multi-core era, workstation clusters have emerged as a cost-effective approach to build a network of workstations (NOWs). NOWs connect the small groups of processors to a network of switching elements that form irregular topologies. Designing an efficient routing and a deadlock avoidance algorithm for irregular networks is quite complicated in terms of latency and area of the routing tables, thus impractical for scalability of On Chip Networks. Many deadlock free routing mechanisms have been proposed for regular networks, but they cannot be employed in irregular networks. In this paper a new methodology has been proposed for efficient routing scheme, called LBDR-UD, which save the average 64.59

Index terms— up*/down*, routing, LBDR, irregular networks, LBDR-UD.

1 Introduction

ulti Processor-SoC (MPSoC) and Chip-Multi Processors (CMP) achieve high performance with interconnection networks that give lowlatency, high-bandwidth inter-processor communication [7]. Most of these multi-core system use regular topologies (such as torus, hypercube and mesh) to link their switch components. For packet transmission, many routing schemes have been design to provide an efficient and deadlock free path [1,2,4,5,8,10]. Routing algorithm (RA) decides the path for the packet from source to destination. Two type of RA i.e. distributed and source routing are used for regular and irregular NoC networks [8]. Source routing compute the whole routing path at the source and computed path stored in the packet header, while in distributed routing each router receives a packet; all computations are performed at the switch level, without storing whole path in packet header and decides the output direction to send it. In recent years, several routing schemes have been proposed for application specific networks (i.e. Irregular networks) [6,9,11,12,13,14,15,16].

schemes are able to route packets in different network topologies and achieves livelock and deadlock freedom. To deal with irregular topologies, table based approaches were proposed. In this scenario, at each switch that stores a table, for each end-node, the output port that must be used. Using this approach higher adaptivity is achieved and several outputs are stored in each table. The main benefit of this type of routing is that any topology and any routing algorithm can be used; it also supports fault-tolerant routing algorithms. With such routing approaches, the size of routing table increases proportionally with the size of the network at each switch. Hence, the implementation becomes comparatively complex for the communication switch.

In this paper a efficient routing algorithm is proposed for irregular networks. The aim is to develop a distributed routing on every switch and remove the tables, the routing decision is made quickly and low latency for packets sending from source to destination. The wormhole switching technique is used in our interconnection networks. The routing algorithm is based on combination of up*/down* and LBDR, and hence called LBDR Up*/Down* (LBDR-UD). [12] up*/down* routing is distributive table-based routing algorithm used in the irregular network and [7] LBDR is a table-less routing implementation technique for regular and irregular networks (generated from the mesh).

2 II.

3 Lbdr-ud Routing for Irregular Networks

We start the description with the basic mechanism required at every switch to deal with the irregular networks.

4 a) Methodology

In order to enable an efficient routing implementation for irregular networks using minimum logic, an example network for irregular Network-on-Chip with core and channels are placed according to the application condition as shown in Fig. 1.

The proposed methodology is based on two assumptions:

i.

The interconnection network between switches can be modeled by a multigraph $G(N, C)$, where N is the group of switches and C is the group of bidirectional links between the switches. These ii. For each irregular networks, applied routing algorithm must follow some restrictions. These restrictions are as follows: a. Deadlock-freedom

The routing algorithm must guarantee that the transmitted messages are received at destination and prevent the deadlock scenarios.

b. Connectivity It is essential that the routing algorithm should be capable to offer at least one route between two end nodes. Routing is based on a direction assignment to the operational links, including the ones that do not belong to the tree. In particular, the "up" direction of each link is defined as: 1) A link leading to a parent node in the spanning tree; 2) A link leading to a lower ID, if both are at the same tree level. The "down" direction is along the reverse direction of the "up" direction as shown in Fig. 2. The routing restrictions for the LBDR-UD routing algorithm are shown in Fig. 2. A routing restriction is defined between two successive channels. The LBDR-UD algorithm prohibits messages from taking "downup" transitions. The transitions are allowed in opposite direction by algorithm, thus routing restrictions does not exist for "up" link to "up" and "down" links. Similarly, no routing restrictions are applicable from "down" link to "down" link transitions.

5 b) Configuration bits

Configuration bits are in two sets: connectivity bits and routing bits. Routing bits specify which routing options can be used, whereas connectivity bits specify connectivity with neighbors.

6 R UU and R UD

These bits indicate that the message can take the "up" direction from the current router and from the next router the message can be transmitted in the "up" direction or the "down" direction respectively.

7 R DD and R DU

These bits indicate that the messages can take the "down" direction from the current router and from the next router the message can be transmitted in the "down" direction or the "up" direction respectively.

Note that the routing restrictions and routing bits are the opposite to each other. Fig 3(a) shows the restricted turns and allowed turns a message could take according to router 10 and its routing bits. Specifically, bit RUD at router 10 is 1(Set) and shows that a message is routed to the "up" direction first and then to the "down" direction from the next router. Routing decision is taken again at the next corresponding router. Table ?? shows the bits computed for an irregular network using the LBDR-UD routing algorithm (connectivity bits can be seen in Fig. 3(b)). As shown in the figure, bit R DU is set to zero, representing the "down" to "up" routing restrictions which "LBDR-UD" imposes. Bits R UU and R DD are all set except for those cases where the message would be routed out of the network (at the root router and leaf router). R UD is set ("up" to "down" transitions are allowed) except for those cases where the message would be routed out of the network.

Finally, based on neighboring routers, connectivity bits are set.

Fig. 4 shows the algorithm in pseudo-code for the computation of configuration bits. Function check link shows that whether a link between current router and neighboring router exist or not. Based on the type of restriction the routing bit is set on behalf of its immediate neighbor router. In the LBDR-UD routing only single turn (RDU) is restricted and rest three turns (RUU, RDD and RUD) are allowed. The propose algorithm is flexible, simple and compact routing mechanism for unicast communication that eliminates the requirement for routing tables at every router. The routing logic is separated in two stages. The first stage computes the location of the relative destination router. A general representation of LBDR-UD routing is shown in Fig. 5 and Fig. ?? Initially a comparator module is used, which generates two control signals using three comparators. First comparator (CMP) is used to compare the current_id_level and Dest_id_level, and if the levels are equal then it compares using the Direct Connection CMP otherwise the Ancestor CMP is used. These signals, U1 and D1 indicate the relative direction of the destination in "up" direction and "down" direction respectively.

For example, in Fig. 2, if the current router is 7 and our destination is router 6, signal U1 would be set, because it is situated at the lower level in comparison with the current router. With the help of these connectivity (C U) bits, routing (R UD) bits and control signals, the LBDR-UD routing generates a set of routing Table ?? : Connectivity bits for an irregular network, Routers are numbered row-wise. (See Fig. 3(b)) The second stage

requires two or more logic units and each logic unit will correspond to one output port. Each output port can be implemented with only one inverters, one OR gate and three AND gates. We describe here the logic associated with the up and down output direction, as shown in figure 3.19. Router C 0 C 1 C 2 C 3 C 4 C 5 C 6 C 7 C 8 C 9 C 10 0 0 1 0 1 0 0 1 0 0 0 0 1 1 0 0 0 0 0 0 0 0 1 1 2 0 0 0 0 0 0 0 1 0 1 0 3 1 0 0 0 0 1 0 0 0 0 1 4 0 0 0 0 0 1 0 1 1 0 0 5 0 0 1 1 1 0 1 0 0 1 0 6 1 0 0 0 0 1 0 1 0 0 0 7 0 0 0 0 1 0 1 0 0 0 1 8 0 0 0 0 1 0 0 0 0 1 1 9 0 1 0 0 0 1 0 0 1 0 0 10 0 1 1 1 0 0 0 1 1 0 0

When any of the falling out three conditions is fulfilled, then the incoming packet is headed in "up" output direction for routing. The "up" direction is not considered for routing the packet when none of the following conditions are fulfilled (additionally, the connectivity bit CU is examine in order to filter the up direction).

- ? The destination is directly connected with destination1 1 D U \times
- ? The destination is the ancestor of source router and the message can take the up direction at the lower level router through the up direction output port UU R U \times 1

8 Results and Analysis

In the following, we provide performance evaluation of LBDR-UD and TABLE based (up*/down*) with different network size. Average memory, latency and throughput are calculated on 10 different scenario of each network size (Total 60 scenarios).

9 a) Effect of Network Size on Memory

Distributed Table based routing schemes have also been proposed to deal with irregular topologies and can be used in application-specific systems which facilitates the use of any topology with any routing algorithm. On small systems the hardware cost and power consumption related to the memories used to build routing tables is affordable, but as more and more cores are integrated on the chip, causing the system

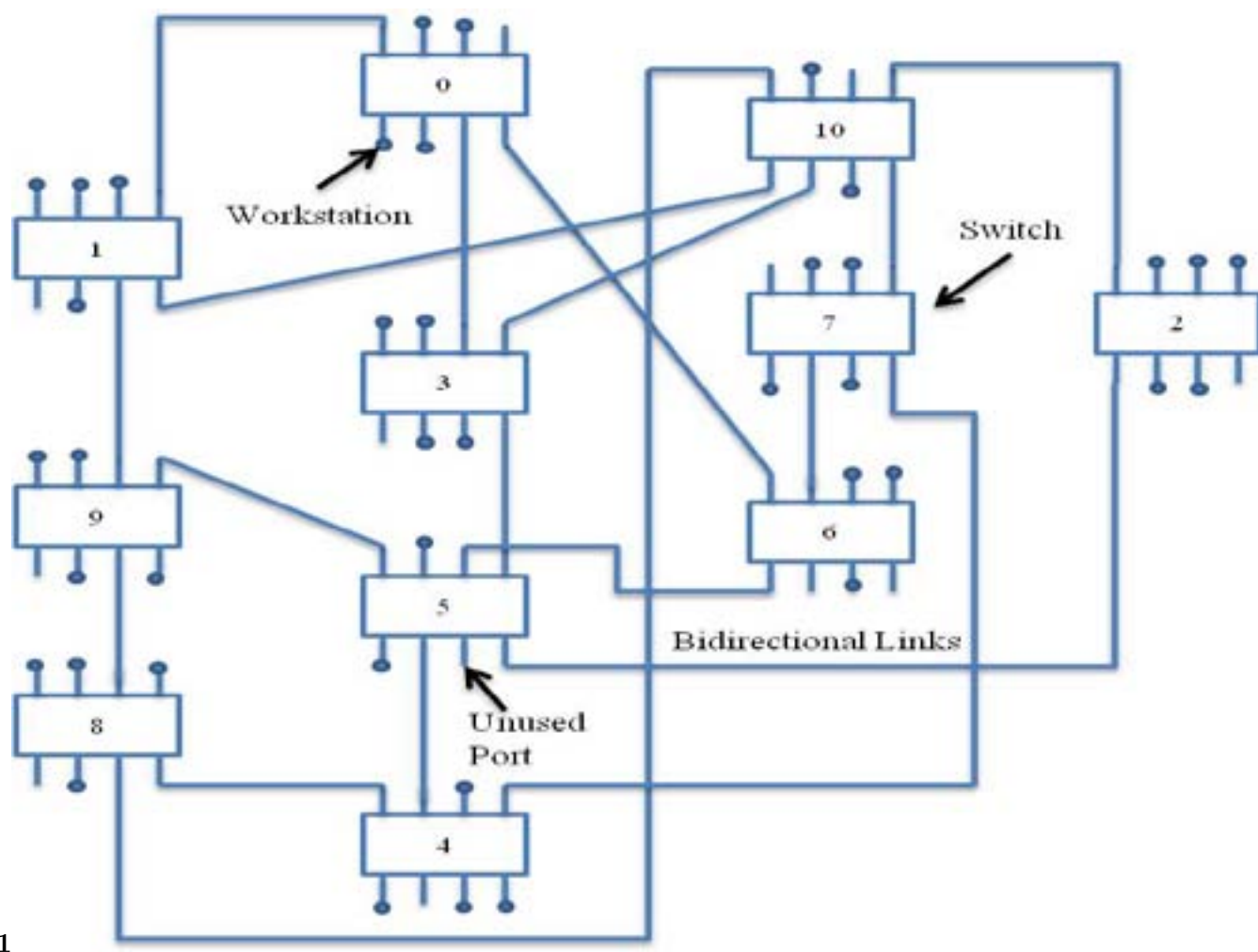
10 Conclusion

It is extension of up*/down* routing in irregular networks using LBDR. LBDR-UD minimizes the memory space of the table based routing (up*/down*) in the NoC for irregular networks. On the behalf of simulation evaluation LBDR-UD save the average 64.59% tables and also efficient in terms of network average latency/flit and throughput/packet as compare to TABLE based (up*/down*) routing.

In application specific topologies (Irregular networks) LBDR also used for 3D irregular networks and this research will be extended by designing the efficient router architecture for NoC. Year 2014 ¹

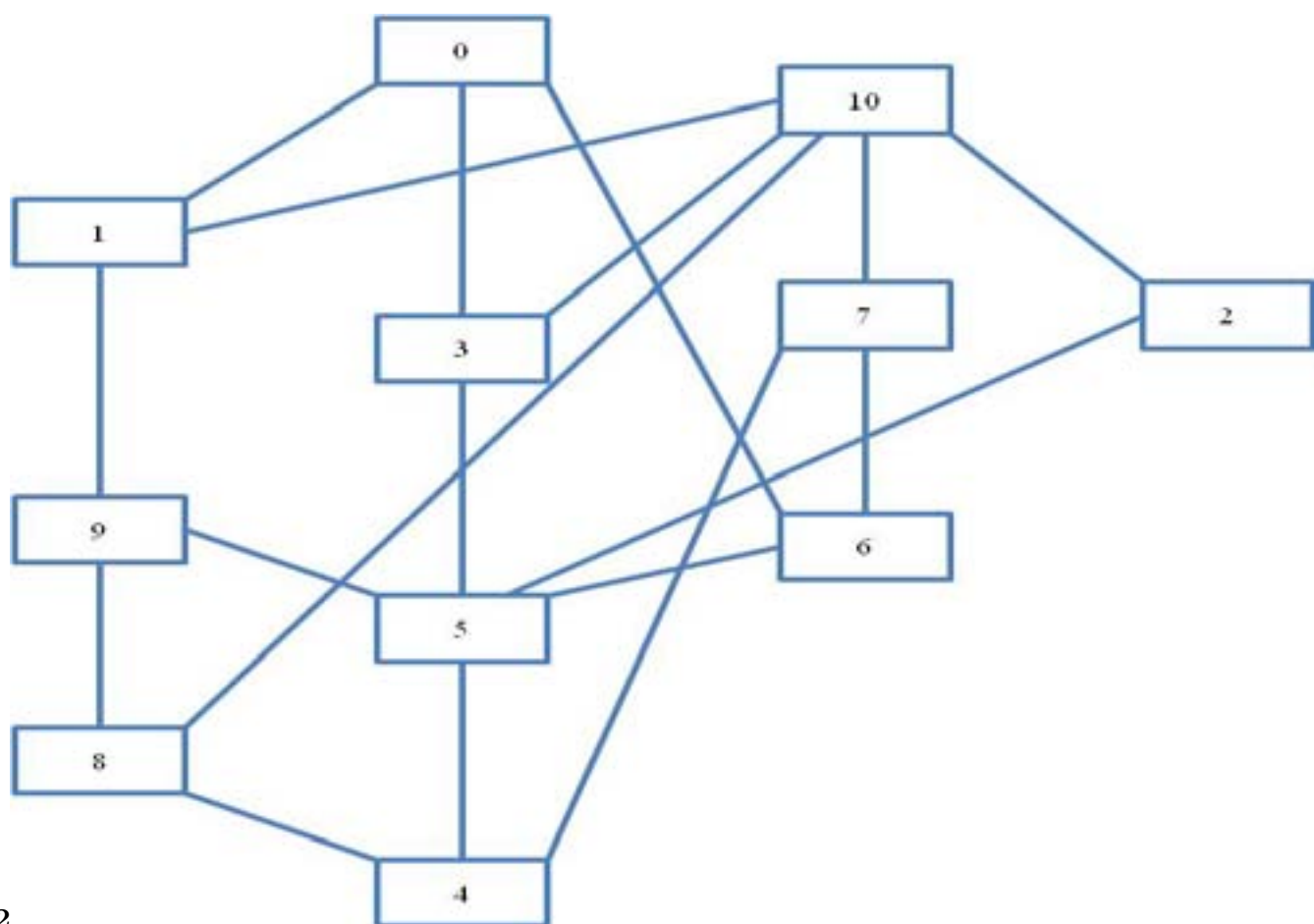


Figure 1: M



1

Figure 2: Figure 1 :



2

Figure 3: Figure 2 :

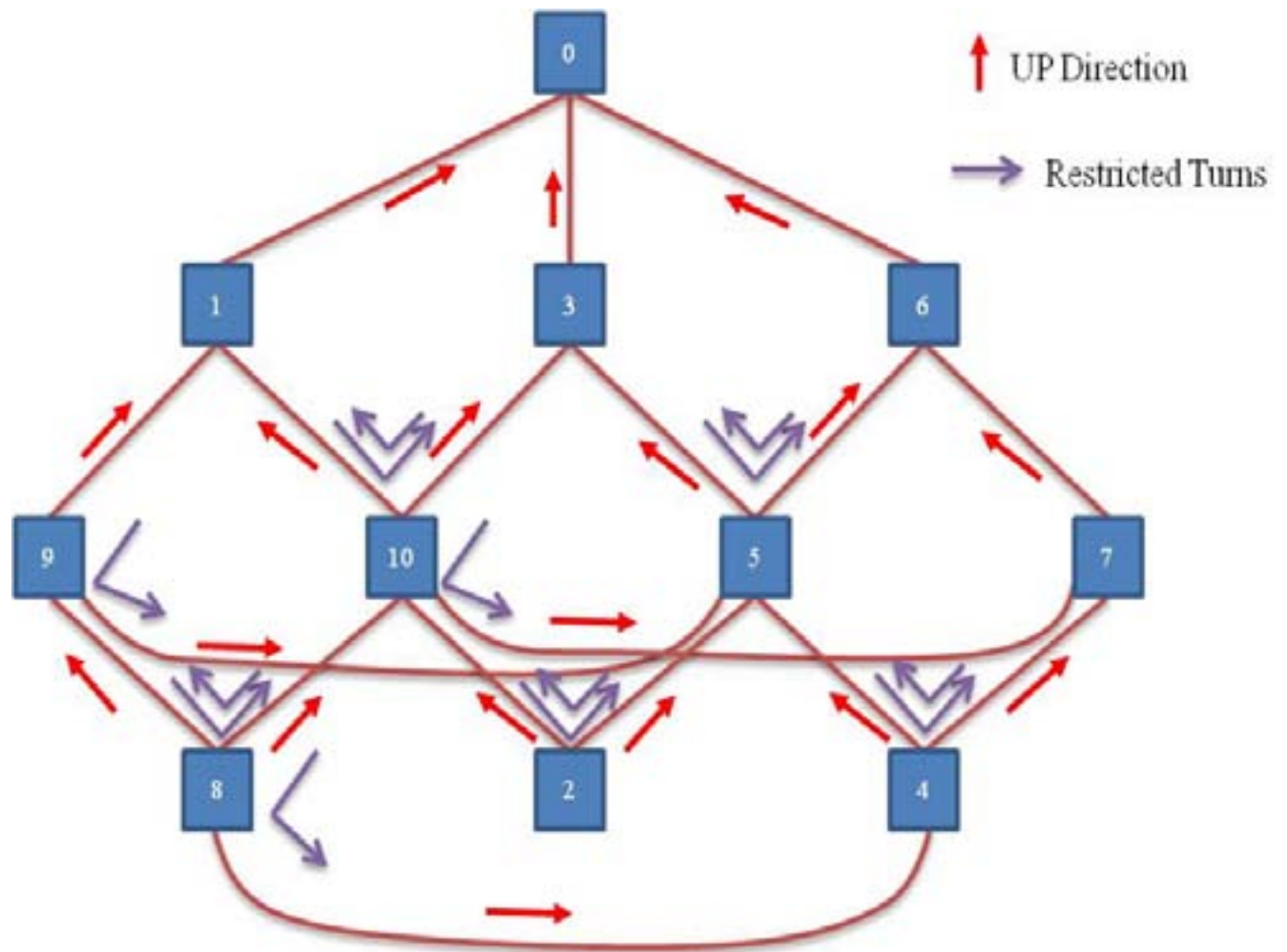
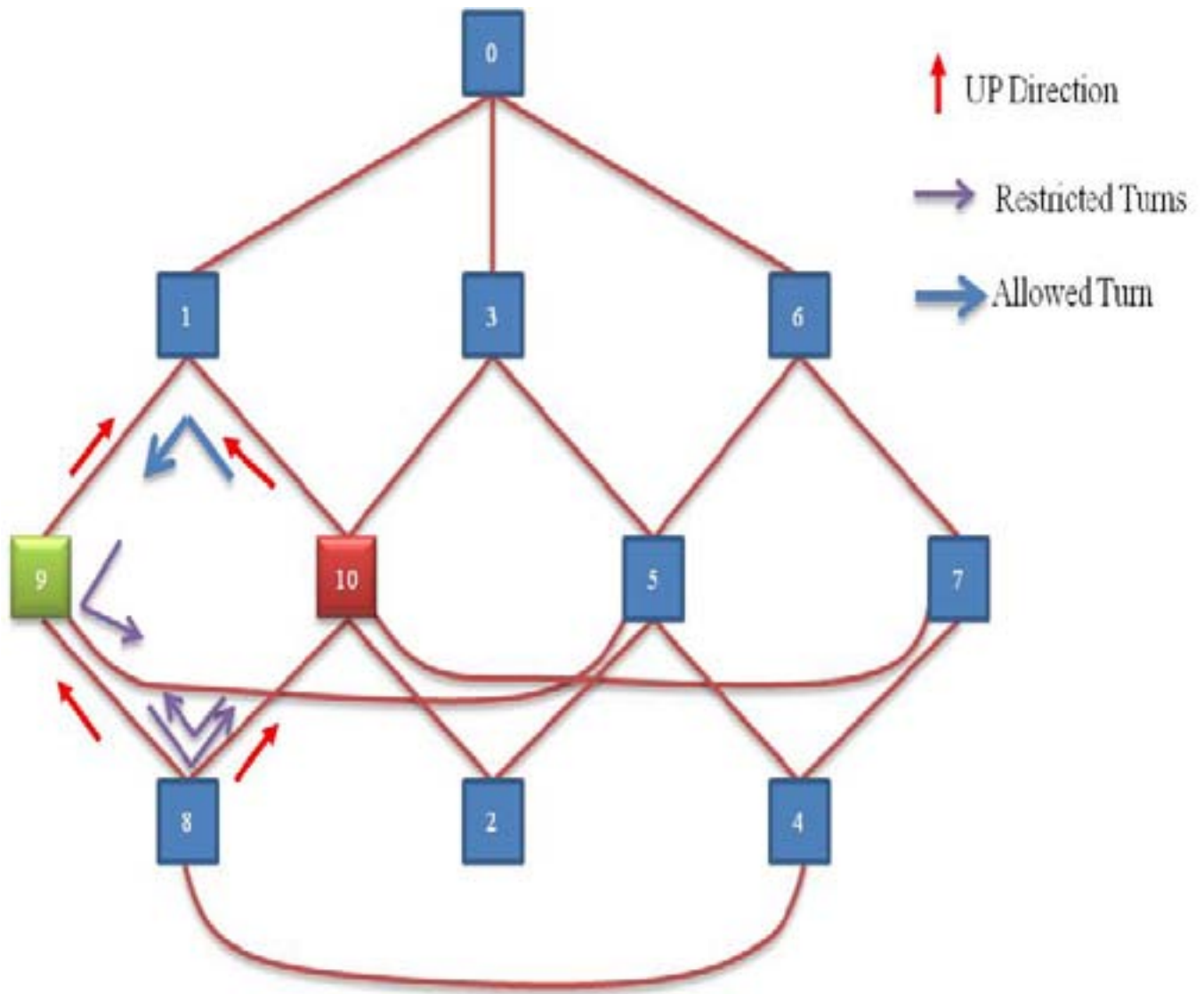
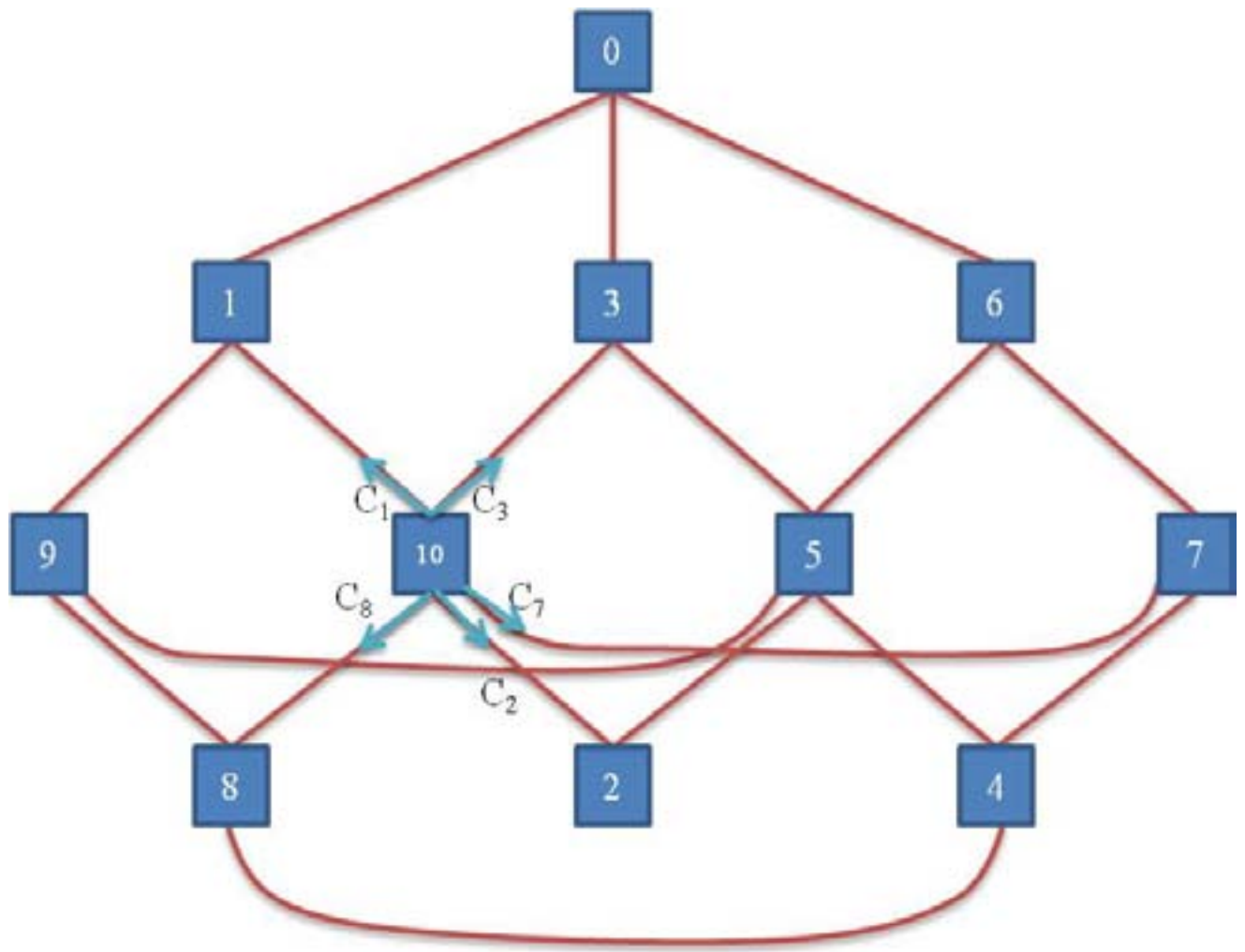


Figure 4: An



3

Figure 5: Figure 3 :



For router 7 , $C_1=C_3=C_8=C_7=C_2=1$

4

Figure 6: Figure 4 :

Input : Topology definition with location of routing restriction and existent links

Output : Configuration bits

Procedure :

//checking connectivity bits of current router

for each router

for (all neighbours of current router)

$C_n = 1$; //connectivity bit of neighbour

end for

for each router //checking restriction, defined as unidirectional

getRouting Restriction(Curr_id);

end for

Figure 7: An

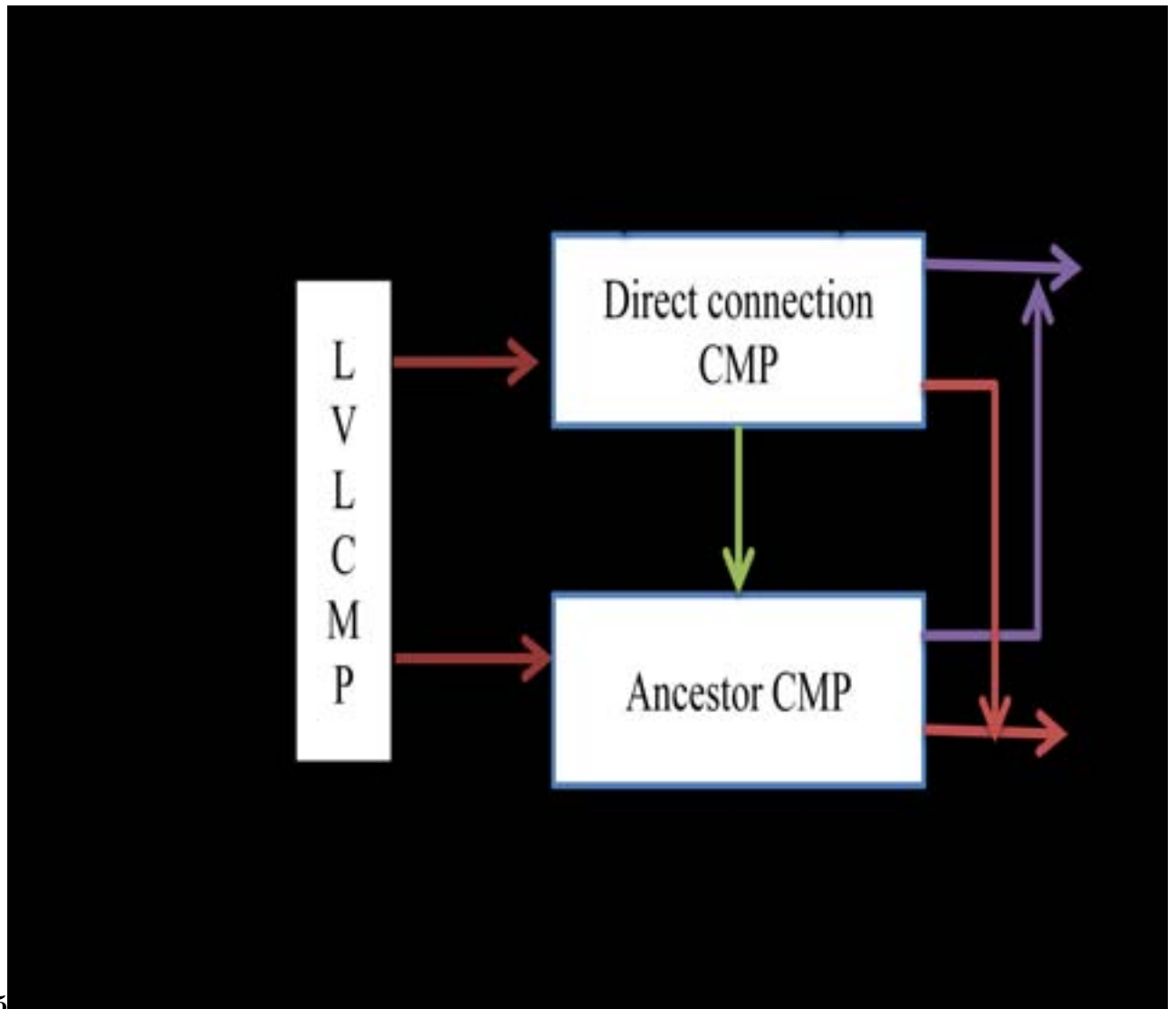


Figure 8: Figure 5 :

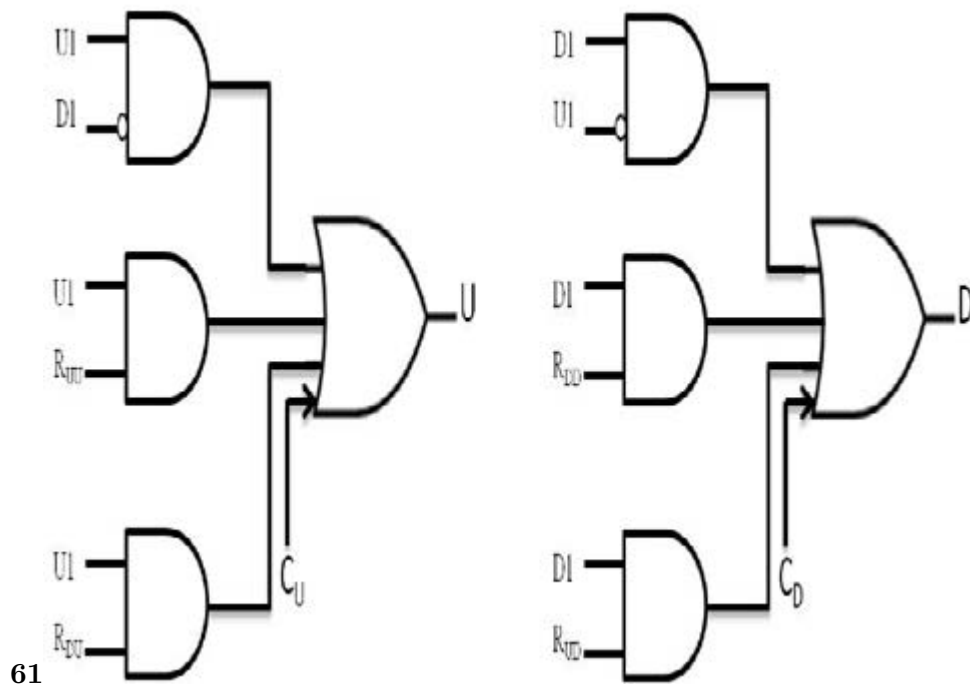


Figure 9: Figure 6 : $\times 1$.

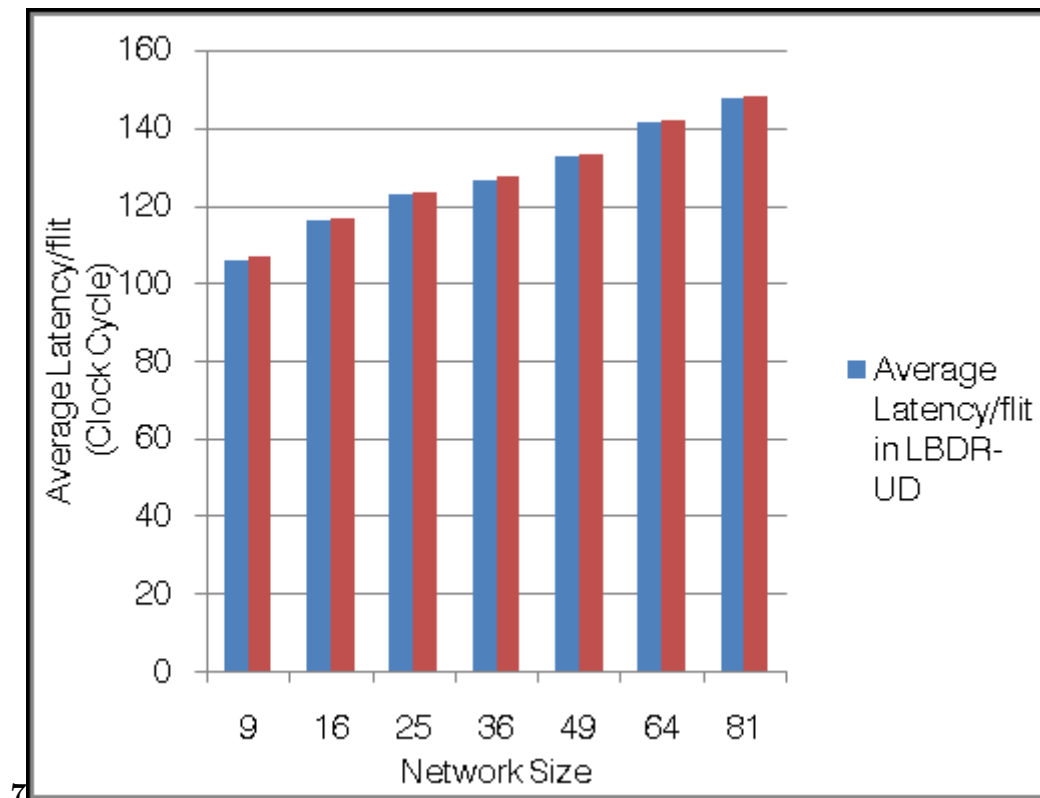


Figure 10: Figure 7 :

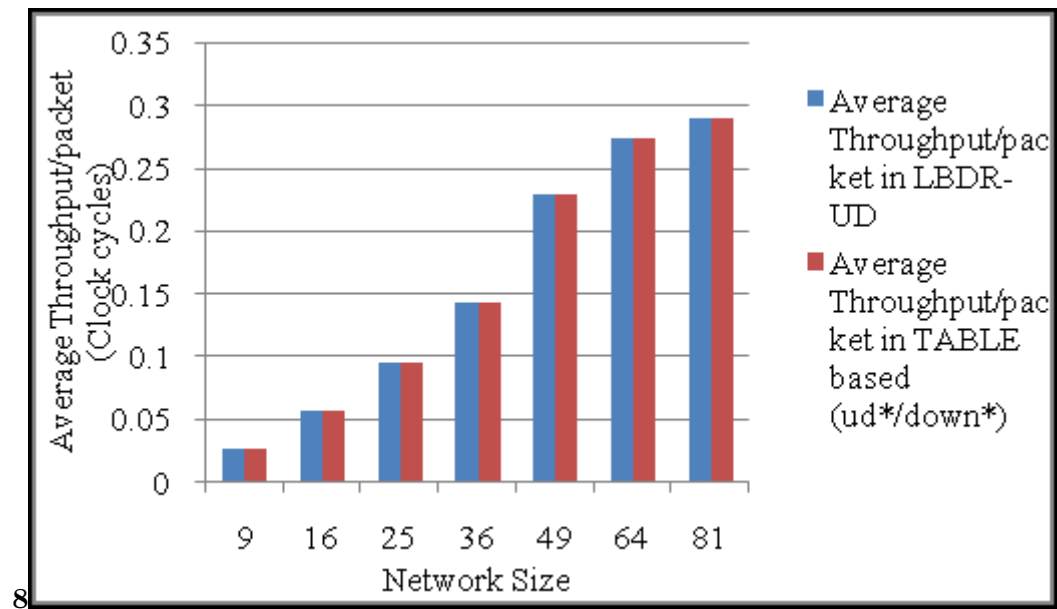


Figure 11: Figure 8 :

Figure 12:

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