



GLOBAL JOURNAL OF COMPUTER SCIENCE AND TECHNOLOGY: A
HARDWARE & COMPUTATION

Volume 16 Issue 1 Version 1.0 Year 2016

Type: Double Blind Peer Reviewed International Research Journal

Publisher: Global Journals Inc. (USA)

Online ISSN: 0975-4172 & Print ISSN: 0975-4350

Design and Analysis of Low Run-Time Leakage in a 13 Transistors Full Adder in 45nm Technology

By Md.Masood Ahmad, Dr. K.Manjunathachari & Dr.K.Lalkishore

GITAM University

Abstract- In this paper a new full adder is proposed. The number of Transistors used in the proposed full adder is 13. Average leakage is 62% of conventional 28 transistor CMOS full adder. The leakage power reduction results in overall power reduction. The proposed full adder is evaluated by virtuoso simulation software using 45 nm technology of cadence tools.

Keywords: peak leakage, average leakage, peak power, average power, 13 transistors full adder, run-time leakage.

GJCST-A Classification: G.4, B.3.2



Strictly as per the compliance and regulations of:



© 2016. Md.Masood Ahmad, Dr. K.Manjunathachari & Dr.K.Lalkishore. This is a research/review paper, distributed under the terms of the Creative Commons Attribution-Noncommercial 3.0 Unported License (<http://creativecommons.org/licenses/by-nc/3.0/>), permitting all non-commercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

Design and Analysis of Low Run-Time Leakage in a 13 Transistors Full Adder in 45nm Technology

Md.Masood Ahmad ^α, Dr. K.Manjunathachari ^σ & Dr.K.Lalkishore ^ρ

Abstract- In this paper a new full adder is proposed. The number of Transistors used in the proposed full adder is 13. Average leakage is 62% of conventional 28 transistor CMOS full adder. The leakage power reduction results in overall power reduction. The proposed full adder is evaluated by virtuoso simulation software using 45 nm technology of cadence tools.

Keywords: peak leakage, average leakage, peak power, average power, 13transistors full adder, run-time leakage.

I. INTRODUCTION

In this paper various 1-bit full adders are considered for leakage analysis. A 13 Transistor Full adder is designed and analysed for low leakage. Full adders considered for analysis in this paper are Complimentary MOS implementation of full adder[29], Mirror full adder [29], Transmission gate full adder[29], Manchester full adder[29], Complimentary pass transistor logic full adder, Low power Full adder, Lean integration with pass transistor full adder, 20 Transistor Transmission gate full adder, Improved 14 transistor Full adder, SERF Full adder, GDI XOR full adder, 10 transistor full adder, 9A full adder, 9B full adder, 13A full adder, 8 transistor full adder and proposed 13 transistor full adder. full adders and their implementation style at transistor level including the proposed full adder is as follows.

CMOS Transistor Full Adder: Conventional CMOS Full Adder consists of 28 transistors as shown in fig.1. From the following equations one can design CMOS 28 Transistor full adder circuit[29].

$$C_o = AB + [A + B]C \quad (1)$$

$$S = ABC_i + C_o(A + B + C_i) \quad (2)$$

Mirror Adder: The fig.2. shows Mirror Adder. An improved adder circuit, also called as "Mirror Adder"[2]. This is a clever implementation of the propagate/generate/delete function when either D or G is high, CO is set VDD of Gnd, respectively. When the conditions for propagate are valid (or P is 1), the incoming carry is propagated to CO.

Author α: School of Technology ECE, GITAM University Rudrarum, patancheru Medak-502329. e-mail: masoodahmad80@gmail.com

Author σ: School of Technology, ECE, GITAM University Rudrarum, patancheru Medak-502329. e-mail: manjunath.gitam@rediffmail.com

Author ρ: Former Vice chancellor JNTUA, CVR college of engg, Hyd. e-mails: lalkishorek@yahoo.com, lalkishorek@rediffmail.com

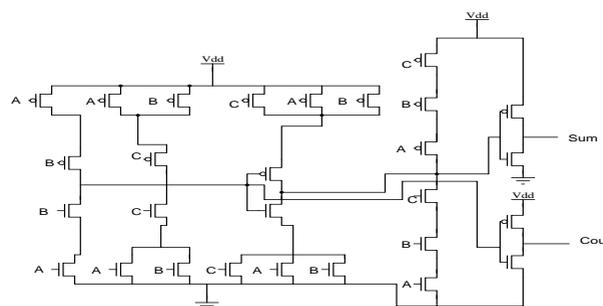


Figure 1: Transistors Full Adder

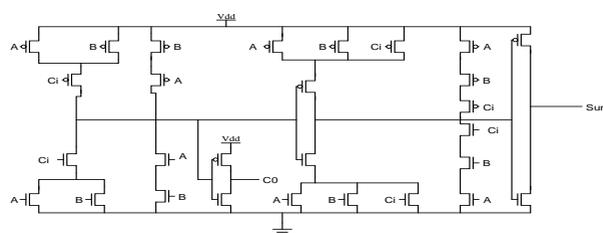


Figure 2: Mirror Adder[29]

Transmission Gate Full Adder: A full adder can be designed to use MUX and XOR. While this impractical in a complementary CMOS implementation, it becomes attractive when MUX and XORs are implemented as transmission gates[4]. The Transmission Gates Full Adder is as shown in fig.3.

Manchester Full Adder: The main idea of designing this adder is to optimize carry chain till some extent in TG full adder by adding generate and delete signals[5]. The propagate path is unchanged, and it passes Cin to the Cout output if the propagate signal is true. If the propagation condition is not satisfied, the output is either pulled low by Di signal or pull up by Gi. Manchester Full adder[29] as shown in fig.4.

Complimentary pass transistor logic: The CPL Full Adder has 18 transistors[33] and is based on NMOS passtransistor logic as shown in fig.5 and fig.6.

Low Power Full Adder: This novel adder [43] cell has 16 transistors. It is based on the 4-transistor implementations

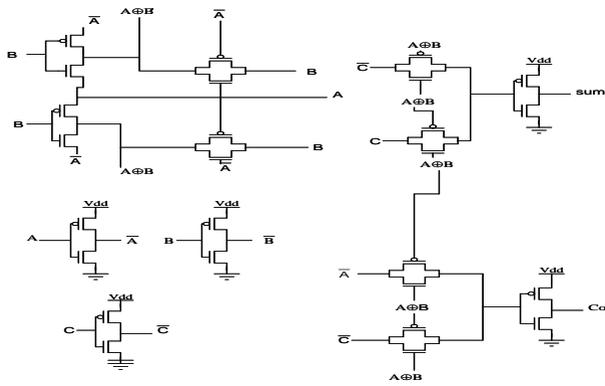


Figure 3: Transmission Gates Full Adder[29]

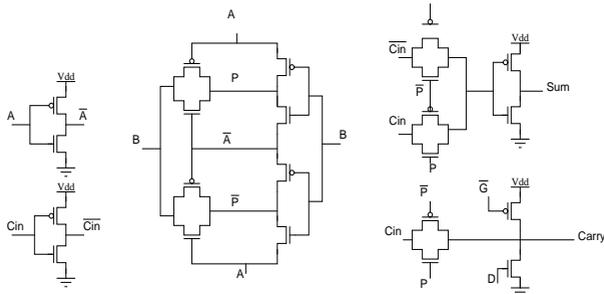


Figure 4: Manchester Static Full Adder[29]

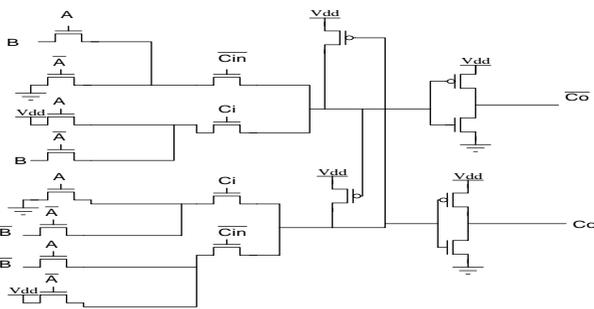


Figure 5: Complementary Pass Transistor Logic Full Adder[33]

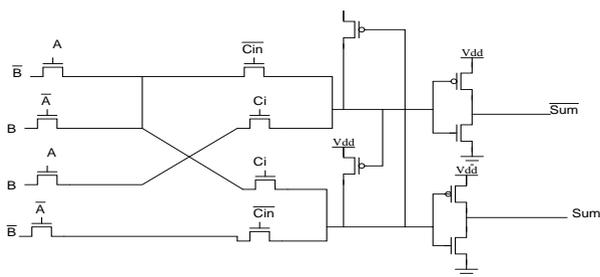


Figure 6: Complementary Pass Transistor Logic Full Adder[33]

of the XOR and XNOR functions. The LP adder is as shown in fig.7.

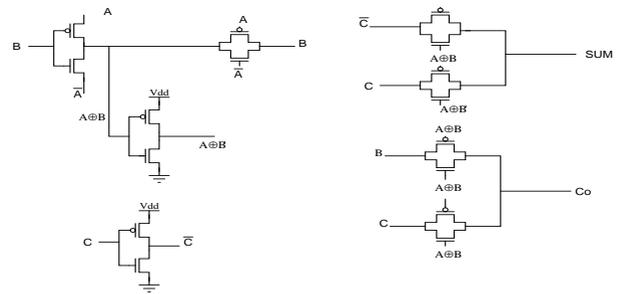


Figure 7: Low Power Full Adder[43]

LEAP Full Adder: The pass transistor based cell library and synthesis tool are constructed to clarify the potential of top down pass transistor logic. The entire scheme is called LEAP[43] (Lean Integration with Pass-transistor). The LEAP Full adder is as fig.8.

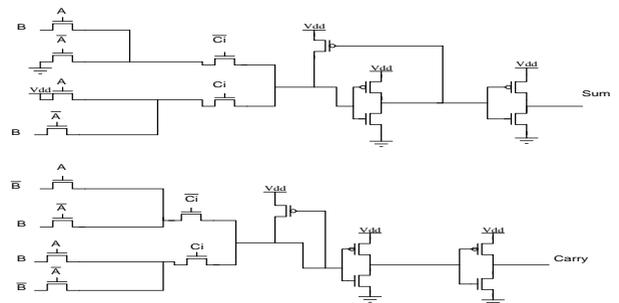


Figure 8: LEAP Full Adder[43]

20 Transistor Transmission Gate Full Adder: Transmission gate approach[36] which is another widely used CMOS design style to implement digital function has been discussed. Transmission gate based implementation is similar to pass transistor with the difference that transmission gate logic uses NMOS and PMOS transistors where as pass transistor logic uses only one type of transistor i.e. either NMOS or PMOS. 20 Transistor Transmission Gate Full adder is as shown in fig.9.

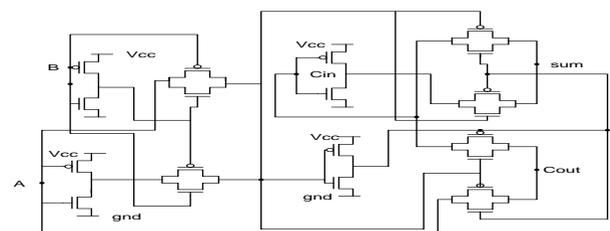


Figure 9: 20T Transmission Gate Full Adder[36]

Improved 14 Transistor Full Adder: The 14T full adder [40] contains a 4T PTL XOR gate an inverter and two transmission gates based multiplexer designs for Sum and Cout signals as shown in fig.10. The circuit is simpler than the conventional adder. This circuit has 4 transistor XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used simultaneously

to generate Sum and Cout. 14 Transistor full adder is as shown in fig.10.

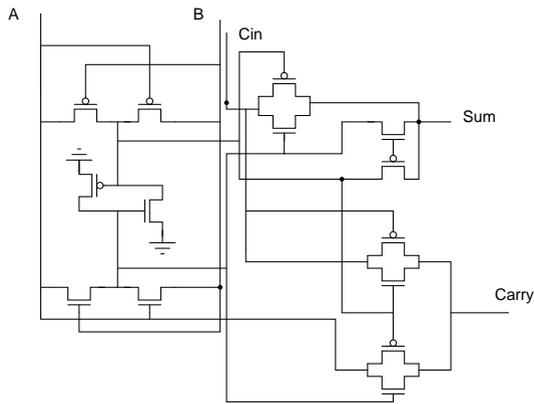


Figure 10: 14T Full Adder[40]

SER Full Adder: SERF adder[11] reuses charge by the energy recovering logic and hence consumes less power than non-energy recovering logic. SERF adder has no direct path to the ground, therefore power dissipation is reduced. The charge stored at the load capacitance is reapplied to the control gates. The joint effect of these two things makes the SERF adder an energy efficient design. SERF Full adder as shown in fig.11.

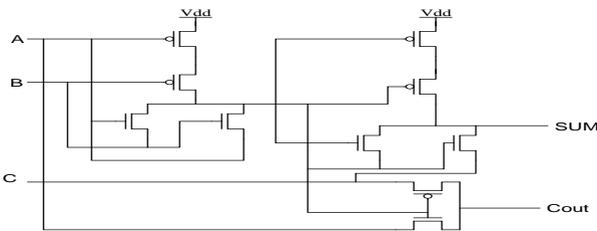


Figure 11: Static Energy Recovery Full Adder[11]

GDI XOR Full Adder: GDI[39] technique is implemented to design a high performance and low power full adder. GDI cell contains three inputs- G (common state input of NMOS and PMOS), N (input to the source or drain of NMOS) and P (input to the source or drain of PMOS). GDI XOR Full adder as shown in fig.12.

10 Transistor Full Adder: Full adder using 10T uses more than one logic style for the implementation and it is called as Hybrid logic design style. The number of transistors count is 10. 10 Transistor Full adder[41] is as shown in fig.14.

9A Full Adder: The 9A Full adder[38] shown in below figure implemented using four transistor static energy recovery XNOR, four transistor ground less XNOR and 2:1 multiplexer. 9A Full adder as shown in fig.15.

9B Full Adder: It resembles the inverter-based XOR but the difference is that the Vdd connection in the inverter based XOR is connected to the input A. Since the new

XOR gate has no power supply, it is called Powerless XOR, or PXOR. A new XNOR gate is named as Groundless XNOR or GB

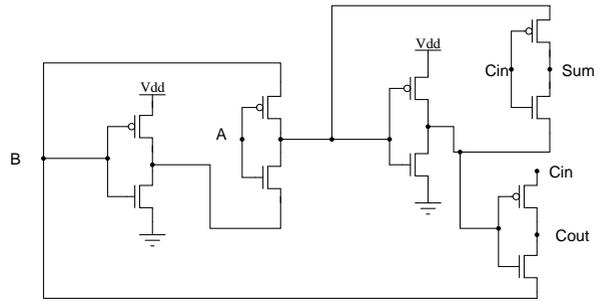


Figure 12: Gate diffusion XOR Full Adder[39]

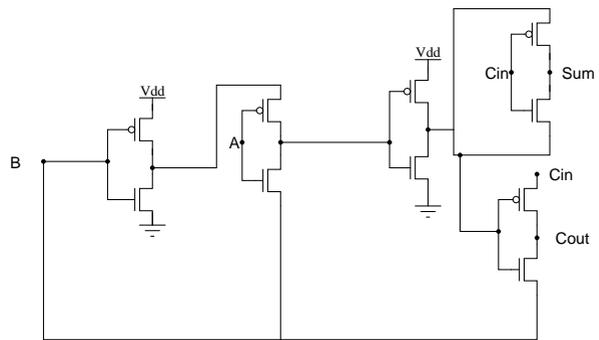


Figure 13: Gate diffusion XNOR Full Adder[39]

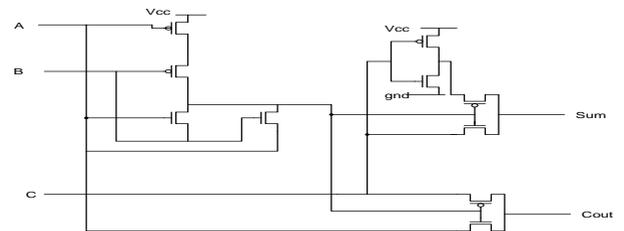


Figure 14: 10T Full Adder[41]

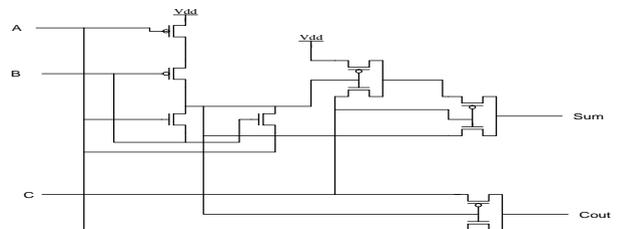


Figure 15: 9A Full Adder[38]

XNOR because there is no direct connection with ground. 9B Full adder[38] is as shown in fig.16.

13A Full Adder: The other type of 10 transistors 1-bit full adder is 13A full adder, which have better critical delay than the 10 transistors SERF full adder in all loading conditions. 13A adder[11] comes out as best when compared with respect to low power and delay. 13A adder is built using SERF XNOR and INV XNOR. The

Cout is designed using multiplexer. 13A Full adder is as shown in fig.17.

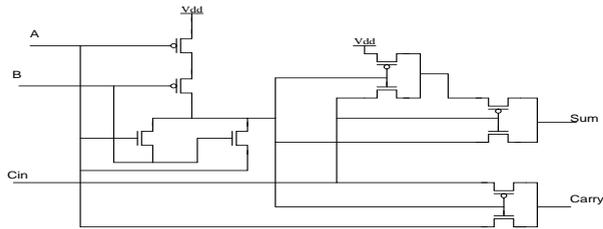


Figure 16: 9B Full Adder[38]

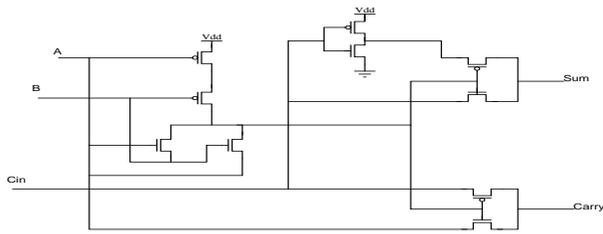


Figure 17: 13A Full Adder[11]

8 Transistor Full Adder: It is built using three multiplexers and one inverter[42]. The inverter in the circuit speeds up propagation of Cout and also provides complemented Cout signal required for generation of Sum. The xor gate is replaced by xnor gate. So the need for inverter is avoided. This reduces the transistor count to 8. The transistor level implementation of the eight transistor full adder is shown in fig.18.

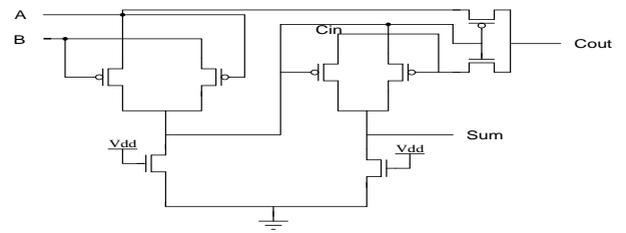


Figure 18: 8T Full Adder[42]

Proposed 13 Transistors Full Adder: After having detail analysis we started to work by undertaking different approach so that we can reduce leakage till some extent along with increase in swing and reduce in average power. Then initially we started on investigating on output swing and came to know that by replacing A_B it is possible to increase the swing as well as decrease in leakage along with average power. It differs from complementary CMOS in that the source side of the MOS transistor is connected to an input line instead of being connected to power lines. Another important difference is that only one PTL network (either NMOS or PMOS) is sufficient to perform the logic operation. In this circuit sum is calculated from output carry. This proposed full adder resulted low leakage as well as low power as comparing with existed full adder.

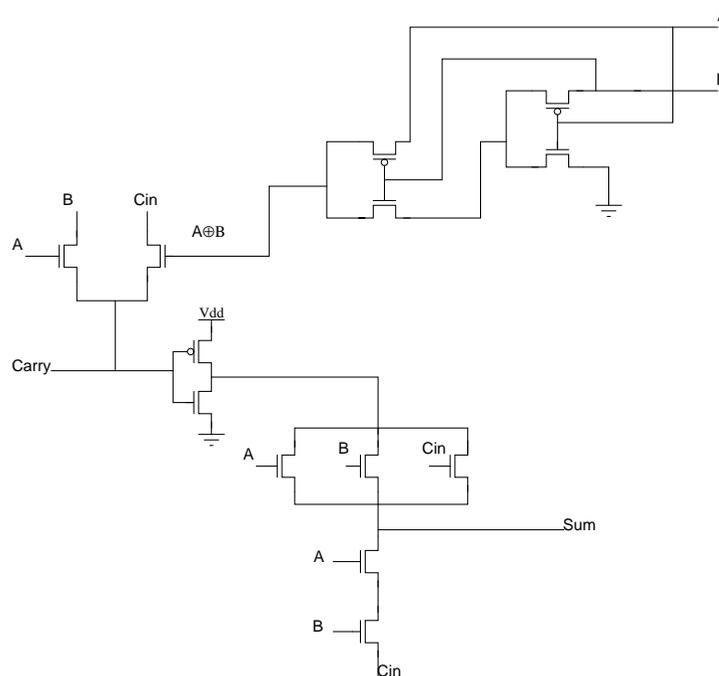


Figure 19: Proposed 13T Full Adder

II. SIMULATION RESULTS

Simulation results are presented in table I for the analysis. The table I shows the comparison of average leakage power, peak leakage power, average power and

peak power in 28 Transistor full adder, Mirror, TG, Manchester, CPL, LEAP, 20T, 14T, SERF, GDI XOR, GDI XNOR, 10T, 9A,9B, 13A, 8T and proposed 13 Transistors full adders.

Table 1: Comparison Of Proposed Full Adders With Existing Full Adders

| Full Adders | Average Leakage | Peak Leakage | Average Power | Peak Power |
|--------------|-----------------|--------------|---------------|------------|
| 28T | 313.2nW | 34.83uW | 351.1nW | 36.26uW |
| Mirror | 288.3nW | 37.48nW | 317.0nW | 28.75uW |
| TG | 8.9uW | 53.80uW | 41.96uW | 69.14uW |
| Manchester | 9.01uW | 76.24uW | 42.32uW | 115.32uW |
| CPL | 27.86uW | 72.52uW | 39.83uW | 63.03uW |
| LP | 9.13uW | 44.14uW | 35.19uW | 54.44uW |
| LEAP | 29.05uW | 73.88uW | 38.42uW | 73.75uW |
| 20T | 11.91uW | 44.62uW | 24.05uW | 41.31uW |
| 14T | 7.04uW | 18.6uW | 720nW | 51.89uW |
| SERF | 2.03uW | 33.31uW | 14.5uW | 29.55uW |
| GDI XOR | 158nW | 10.90uW | 252nW | 24.56uW |
| GDI XNOR | 151.8nW | 15.53uW | 330.4nW | 16.18uW |
| 10T | 7.83uW | 31.97uW | 12.55uW | 31.90uW |
| 9A | 12.48uW | 24.96uW | 116.1nW | 29.35uW |
| 9B | 85.78nW | 33.95uW | 12.45uW | 27.39uW |
| 13A | 8.8uW | 38.14uW | 21.17uW | 43.03uW |
| 8T | 15.76uW | 34.95uW | 20.36uW | 31.91uW |
| Proposed 13T | 196.4nW | 17.10uW | 12.67uW | 52.70uW |

III. CONCLUSION

Below 70 nm technologies run-time leakage power dominates the dynamic power. So one should come up with new full adder which consumes less leakage power compared to dynamic power one such attempt is discussed in this paper.

IV. ACKNOWLEDGMENT

My sincere thanks to my guides Dr. K. Manjunathachari and Dr. K. Lalkishore for their valuable support and encouragement.

REFERENCES RÉFÉRENCES REFERENCIAS

- Shiv Shankar Mishra, Adarsh Kumar Agrawal and R. K. Nagaria "A comparative performance analysis of various CMOS design techniques for XOR and XNOR circuits", International Journal on Emerging Technologies, ISSN : 0975-8364.
- Saradindu Panda, A. Banerjee, B. Maji, Dr. A. K. Mukhopadhyay, "Power and Delay Comparison in between Different types of Full Adder Circuits", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, ISSN: 2278 - 8875.
- Fengbo Ren, and Dejan Markovi, " True Energy-Performance Analysis of the MTJ-Based Logic-in-Memory Architecture ", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL:57, NO:5, MAY 2010.
- Shivshankar Mishra, V. Narendar, Dr. R. A. Mishra, " On the Design of High-Performance CMOS 1-Bit Full Adder Circuits", International Conference on VLSI, Communication and Instrumentation, 2011.
- Walid Ibrahim1, Azam Beg1 and Valeriu Beiu , " Highly Reliable and Low- Power Full Adder Cell", IEEE International Conference on Nanotechnology, August 15-18, 2011.
- Subodh Wairya, Rajendra Kumar Nagaria, Sudarshan Tiwari, "New Design Methodologies for high speed mixed mode CMOS Full adder circuits", International Journal of VLSI design and Communication Systems, Vol.2, No.2, June 2011.
- Subodh Wairya, Rajendra Kumar Nagaria and Sudarshan Tiwari, " Comparative Performance Analysis of XOR-XNOR Function Based High-Speed CMOS Full Adder Circuits For Low Voltage VLSI Design", International Journal of VLSI design and Communication Systems, Vol.3, No.2, April 2012.
- Sumeer Goe, Ashok Kumar, Senior Member, and Magdy A. Bayoumi, " Design of Robust, Energy-Efficient Full Adders for Deep Submicrometer Design Using Hybrid-CMOS Logic Style ", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 14, NO. 12, Dec 2006.
- Subodh Wairya, Rajendra Kumar and Sudarshan Tiwari, "Performance Analysis of High Speed Hybrid CMOS Full Adder Circuits for Low Voltage VLSI Design", Hindawi Publishing Corporation VLSI Design, Volume 2012, Article ID 173079.
- Anu Tonk, Shilpa Goyal, "A Literature Review on Leakage and Power Reduction Techniques in CMOS VLSI Design", International Journal on Recent and Innovation Trends in Computing and Communication, ISSN: 2321-8169.
- Ahmed M. Shams and Magdy A. Bayoumi, "A Novel High-Performance CMOS 1-Bit Full-Adder Cell",

- IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, VOL. 47, NO. 5, MAY 2000.
12. Deepa, Sampath Kumar, "Analysis of Low Power 1-bit Adder Cells using different xor-xnor gates", IEEE International Conference on Computational Intelligence and Communication Technology, 2015.
 13. Prof. Vojin G. Oklobdzija, "High-Speed VLSI Arithmetic Units: Adders and Multipliers".
 14. Sansar Chand Sankhyan, "Comparative Study of Different Types of Full Adder Circuits", Sansar Chand Sankhyan Int. Journal of Engineering Research and Applications, ISSN : 2248-9622, Vol. 3, Issue 5, Sep-Oct 2013.
 15. Mr. Kapil Mangla, Mr. Shashank Saxena, "Analysis of various full adder circuit on various parameters for low power", International Journal of Engineering and Technical Research, ISSN: 2321-0869, Volume-3, Issue- 5, May 2015.
 16. Massimo Alioto, Gaetano Palumbo, "Analysis and Comparison on Full Adder Block in Submicron Technology", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 10, NO. 6, Dec 2002.
 17. Aminul Islam, Ale Imran and Mohd. Hasan, "Robust Subthreshold Full Adder Design Technique", International Conference on Multimedia, Signal Processing and Communication Technologies, 2011.
 18. Manoj Duhan, Kusum Dala, Viplove Kumar, "A Study of Full Adder Circuits: from Power and Speed of Operation", An International Journal of Engineering Sciences, Issue June 2014, Vol. 10.
 19. Abdellatif Bellaouar, University of Waterloo and Moha medl. Elmasry, University of Waterloo, "LOW-POWER DIGITAL VLSI DESIGN: CIRCUITS AND SYSTEMS"
 20. Anand Raghunathan NEC USA, Niraj K. Jha, Princeton University, Sujit Dey NECUSA, "HIGH-LEVEL POWER ANALYSIS AND OPTIMIZATION".
 21. Anantha P. Chandrakasan, MIT; Robert W. Brodersen, University of California/ Berkeley, "LOW POWER DIGITAL CMOS DESIGN".
 22. Gary Yeap, "PRACTICAL LOW POWER DIGITAL VLSI DESIGN".
 23. Jan M. Rabaey, University California and Massoud Pedram, University of Southern California; "LOW POWER DESIGN METHODOLOGIES"
 24. MohabAnis and Mohamed Elmasry; "Multi-Threshold CMOS Digital Circuits Managing Leakage Power".
 25. Neil H. E. Weste and David Money Harris; "CMOS VLSI Design: A Circuits and Systems Perspective".
 26. Nikhil Jayakumar, Suganth Paul, Rajesh Garg, Kanupriya Gulati, Sunil P. Khatri; "Minimizing and Exploiting Leakage in VLSI Design".
 27. P.R. Vander Meer, A. Van Staveren, A. H. M. Van Roermund; "LOWPOWER DEEP SUB-MICRON CMOS LOGIC: Sub-threshold Current Reduction".
 28. Pushpa Saini, Rajesh Mehra; "Leakage Power Reduction in CMOS VLSI Circuits"; International Journal of Computer Applications (09758887), Volume 55, No. 8, October 2012.
 29. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic; "Digital Integrated Circuits: Design approach". of IEEE International Conference on Power, Control and Embedded System (ICPES), 28 Nov.-1 Dec. 2010.
 30. Tejaswi Raja, "Minimum Dynamic power CMOS design with variable input delay logic"; May 2004.
 31. Saraju P. Mohanty, Nagarajan Ranganathan, Elias Kougiianos, Priyadarsan Patra; "Low-Power High-Level Synthesis for Nanoscale CMOS Circuits".
 32. Mahmoud and M. Bayoumi, A 10-transistor low-power high-speed full adder cell, in Proc. ISCAS99, Orlando, FL, June 1999, pp. 4346.
 33. K. Roy and S. Prasad, Low-Power CMOS VLSI Circuit Design. New York: Wiley Intersci., 2000.
 34. A. Bellaouar and M. Elmasry, Low-Power Digital VLSI Design: Circuits and Systems. Boston, MA: Kluwer Academic, 1995.
 35. Chandrakasan and R. Brodersen, Eds., Low Power Digital CMOS Design. Boston, MA: Kluwer Academic, 1995.
 36. R. Zimmermann and W. Fichtner, Low-power logic styles: CMOS versus pass-transistor logic, IEEE J. Solid-State Circuits, vol. 32, pp. 10791090, July 1997. A. Shams and M. Bayoumi, A novel high-performance CMOS 1-Bit full-adder cell, IEEE Trans. Circuits Syst. Part II, vol. 47, pp. 478481, May 2000.
 37. J. Wang, S. Fang, and W. Feng, New efficient designs for XOR and XNOR function on the transistor level, IEEE J. Solid-State Circuits, vol. 29, pp. 780786, July 1994.
 38. H. T. Bui, A. K. Al-Sheraidah and Y. Wang, Design and Analysis of 10-transistor Full Adders using Novel XOR-XNOR Gates, Proceedings of ICSP 2000.
 39. A. Morgenshtein, A. Fish and A. Wagner, Gate-Diffusion Input (GDI): A Power-Efficient Method for Digital Combinational Circuits, IEEE Trans. VLSI Syst., pp. 566-581, Oct. 2002.
 40. Shams, A.M. and M.A. Bayoumi, 2000. A novel high performance CMOS 1-bit full adder cell, IEEE Trans. Circuits and Systems-II: Analog digital Signal Process, 47(5): 478-481.
 41. H. T. Bui, Y. Wang, and Y. Jiang, Design and Analysis of 10- Transistor Full Adders Using XOR-XNOR Gates, IEEE Trans. Circuits and Syst. II, Analog Digit. Signal Process., vol 49, no. 1, pp. 25-30, Jan. 2002.
 42. D. Garg and M. K. Rai / IJECCT 2012, Vol. 2 (4) CMOS Based 1-Bit Full Adder Cell for Low-Power Delay Product.
 43. Top-down pass-transistor logic design K. Yano; Y. Sasaki; K. Rikino; K. Seki IEEE Journal of Solid-State Circuits.

44. Chang, C.H., J. Gu and M. Zhang, A review of 0.18um full adder performances for tree structure arithmetic circuits, IEEE Trans:Very Large scale Integration (VLSI) System, vol. 13 (6), pp. 686- 695, 2005.
45. M.Alioto, G.Di Cataldo and G.Plumbo, Mixed Full Adder topologies for high- performance low-power arithmetic circuits, Microelectronics Journal, vol. 38, pp. 130-139, 2007.
46. Adarsh Kumar Agrawal, Shivshankar Mishra, and R. K. Nagaria, Proposing a Novel Low-Power High-Speed Mixed GDI Full Adder Topology, accepted in Proceeding.

