An Efficiency Study on Fault Tolerent Fir Filters

Augusta Angel M[1]

[1] VV COLLEGE OF ENGINEERING

Received: 16 December 2016 Accepted: 4 January 2017 Published: 15 January 2017

Abstract

In this Digital World, Digital filters are the boom for modern digital communications in which Fir filters play a vital role. But the reliability of these filters is still a paradox. Nowadays electronic devices with multiple numbers of filters are used in various fields. Hence the performance and reliability of the filters must be improved. A number of techniques have been introduced to detect and correct errors that occur in those filter circuits. In this paper, the use of hamming code error correction technique on 4 tap fir filters are studied in order to obtain optimized and efficient reliability.

Index terms—

1 I. Introduction

n analog and digital communication fields, the Digital Filters play a vital role. The main purpose of using the filters is to remove the unwanted signal components in order to produce the better quality signal at the output. Figure 1 shows the functional block of digital filter. The digital filter is a discrete system, and it can do a series of mathematic processing to the input signal, and therefore obtain the desired information from the input signal. while compared with the analog filters, the digital filters have unique characteristics of generating the stabilized signal at the output. So that the digital filters are preferred than the analogue one in electronic circuits. The two major classification of digital filters are FIR (Finite Impulse Response) and IIR (Infinite Impulse Response) filter. The FIR filters are employed in filtering problems than IIR filters because of efficient hardware implementation with fewer precision errors and also the stabilized response with the linear phase. Due to its linear phase characteristics, Finite impulse response (FIR) filter plays an vital role in the processing of digital signal.

2 a) FIR Filter Design

Finite-Impulse Response (FIR) filters have considered as important building blocks in many digital signal processing (DSP) systems. The FIR filter is preferred over the IIR filter because of efficient implementation with fewer finite precision error and having better stability with linear phase. In any Fir filter, the output signal is obtained by convoluting the input signal with the filter co-efficient i.e., Data that is either transmitted over communication channel is not completely error free. This change in the data is caused due to external interference, signal distortion, attenuation or from noise. There are two types of errors. Firstly single error in which only one bit is changed. And secondly the burst error in which more than one bits are changed. There are various error detection and correction techniques such as Cyclic Redundancy Checks (CRC), Parity check, LRC, VRC and Hamming Code. This work focuses on Hamming code. A commonly known linear Block Code is the Hamming code. In a block of data, Hamming codes can detect and correct a single bit-error. In these codes, every bit is included in a unique set of parity bits [2]. By analyzing parities of combinations of received bits, the presence and location of a single parity bit-error can be determined. The parities of combinations of received bits are used to produce a table of parities which corresponds to a particular bit-error combination.

This table of errors is called as the error syndrome. If all parities are correct according to this pattern, it can be concluded that there is no single biterror in the message (there may be multiple bit-errors). Due to single bit-error , if there is any error in the parities , the erroneous data bit can be found by adding up the positions of the erroneous parities. Hamming codes are easy to implement. They are generally used in computing, telecommunication, and other applications including data compression, and turbo codes [3]. They are also used for low cost and low power applications.

3 II. Fault Tolerant FIR Filters

To protect a circuit from errors, so many techniques can be used. In the manufacturing process of the circuits, modifications can be done to minimize the number of errors by adding redundancy at the logic to ensure that errors do not affect the system functionality. In signal processing and communication systems, digital filters are most commonly used. More number of techniques has been proposed to protect the circuits. By using number of methods, we can identify the faults and also correct the errors within circuit itself. There are different fault tolerance approaches to conventional circuits and the digital signal processing circuits. Fault tolerant filter implementations are needed, whenever the system reliability is critical. So, using error correction codes, the filters can be protected. Here, we use hamming code for error correction.

The fault tolerant of fir filters are achieved by including the ecc in the fir architecture. Hence if the filter produces a error at the output, it can be detected and corrected by using the error correction unit. Figure 3 depicts that the output of fir filter is given to the error correction unit in which the errorous bit is identified and it is corrected. The error correction unit includes the hamming encoder and decoder. (the positions in an 21-bit sequence that are powers of 2). The parity bit pl is calculated using all bits positions whose binary representation includes a 1 in the least significant position. p2 bit is calculated using all the bit positions with a 1 in the second position and so on. Thus, the parity bits are generated for different combination of bits. The various combinations are: p: bits 1,3,5, 7, 9, 11, 13,15, 17, 19, 21 p2: bits 2, 3, 6, 7, 10, 11, 14, 15, 18, 19 p3: bits 4, 5, 6, 7 ,12, 13, 14, 15, 20, 21 p4: bits 8, 9, 10, 11, 12, 13, 14, 15 p5: bits 16, 17, 18, 19, 20, 21 Figure 4 shows the hamming encoding technique, it shows how the parity bits are included in the data bits. If there is any error on input data bits it can be detected and corrected by using these parity check bits. Table **??** shows the position of error bits based on the parity check bits. For example, an error on d1 will cause errors on the three parity check bits p1, p3; an error on d2 will affect only p2 and p3; an error on d3 will affect only on p1,p2 and p3 and so on. Hence, once the erroneous bit is identified, it is corrected by simply inverting that bit.

4 Table I: Position of error bit

Suppose a binary data 0000001000000100 is to be transmitted, it is encoded by adding redundancy bits in their corresponding position. Now, the encoded data 0000001000000100 will be transmitted to the receiver. The error detection and correction are shown in figure 5. If bit position 14 has been changed from 1 to 0 (i.e, 000000000000010100000)in transmitted data, Then the data will be erroneous. At the receiver side, the hamming decoder recalculates the same set of bits used by sender plus the relevant parity (p) bit for each set. The recalculated value of p5 p4 p3 p2 p1 is 01110, which corresponds to decimal 14. Therefore bit position 14 contains an error. To correct this error, bit position 14 is reversed from 0 to 1.

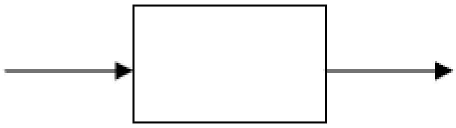
III.

5 Results And Discussion

The described structure has been implemented by using verilog HDL. The error dectection and correction are verified using the Xilinx 13.4 software tool. Figure 6 shows the RTL schematic of fault tolerant fir filter. For example figure 7 shows a output in which a error at the 4 th bit of the transmitted signal is detected by the syndrome (s1) and it is corrected by the error correction unit at the output. Now the error free signal is obtained as a output. By this way the reliability of the system is improved. Figure 8 shows the signal with no error. Since the Syndrome (s1) is 0000, no error is detected. Hence it is transmitted without any correction.

6 Conclusion

Filters are widely used in various digital signal processing applications. Protecting filters from errors is an important task which is addressed by various techniques. In this paper, a study was done on protecting errors by using error correction codes. The hamming code technique is employed along with fir filters, the error which arise due to any fault in the circuits are detected and corrected by this hamming encoder and decoder. The study shows that the reliability of the filters are improved by using this fault tolerant module and it also improves the performance by reducing the area complexity, delay and power. [1] [2]



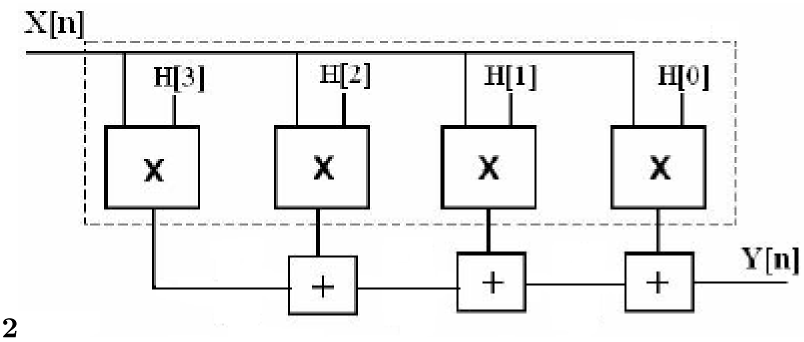
1

Figure 1: Figure 1 :

$$y[n] = x[n] ** h[n] = \sum_{k=0}^{N-1} x[k]h[n-k]$$

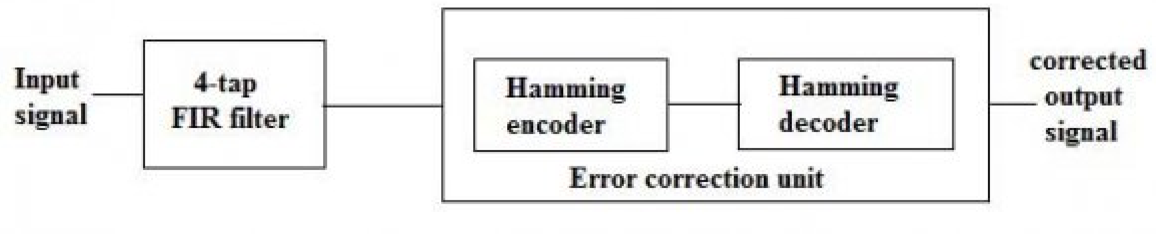
2

Figure 2: Figure 2 :



2

Figure 3: Figure 2 :



3

Figure 4: Figure 3 :

21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
d15	d14	d13	d12	d11	p5	d10	d9	d8	d7	d6	d5	d4	p4	d3	d2	d1	p3	d0	p2	p1
Position of Redundancy bits in Hamming code																				
Data: 0000001000000100																				
21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0	0	0	0	0		0	1	0	0	0	0	0		0	1	0		0		
Adding p1																				
0	0	0	0	0		0	1	0	0	0	0	0		0	1	0		0		0
Adding p2																				
0	0	0	0	0		0	1	0	0	0	0	0		0	1	0		0	0	0
Adding p3																				
0	0	0	0	0		0	1	0	0	0	0	0		0	1	0	0	0	0	0
Adding p4																				
0	0	0	0	0		0	1	0	0	0	0	0	1	0	1	0	0	0	0	0
Adding p5																				
0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0
Encoded data : 000000010000010100000																				

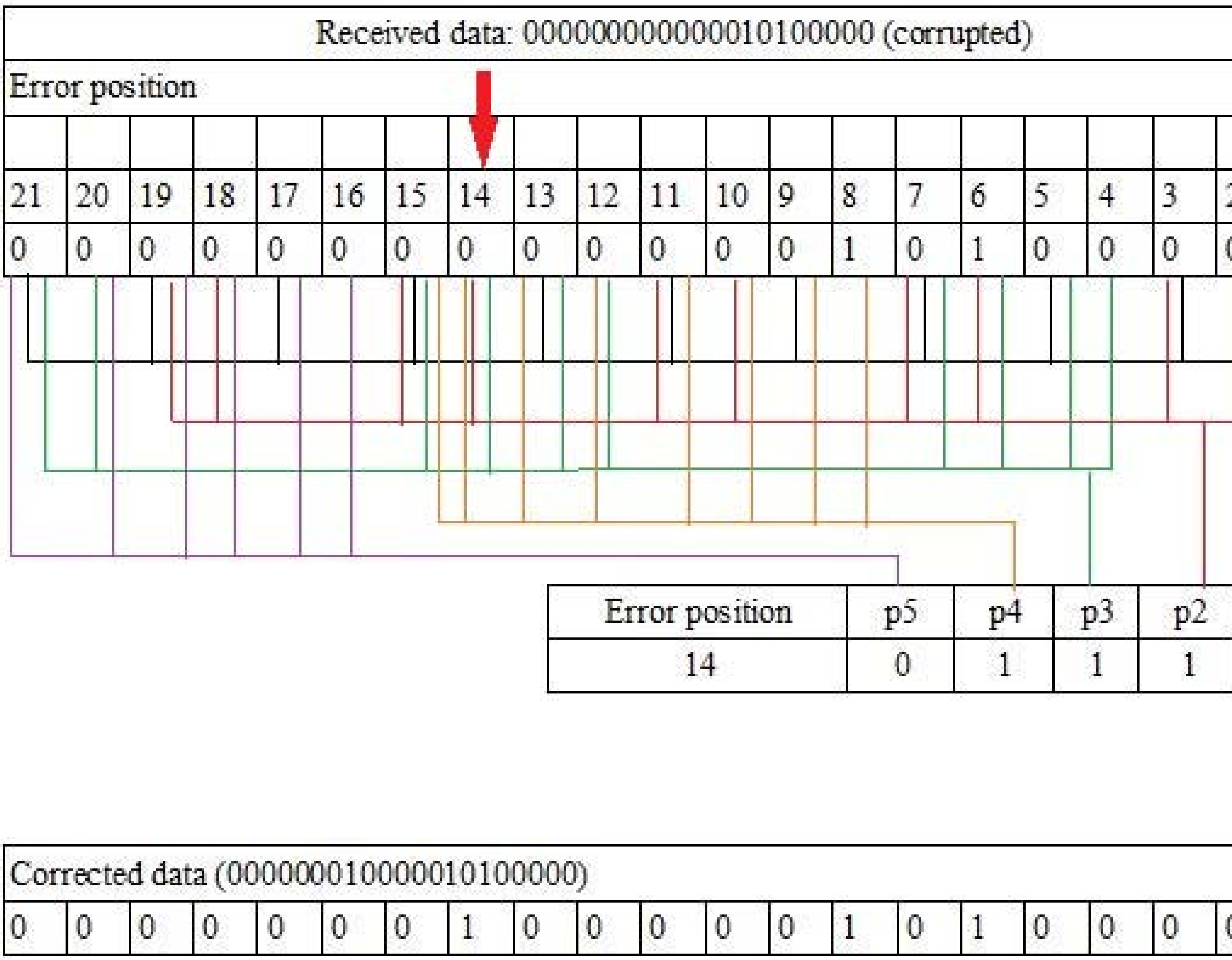
4

Figure 5: Figure 4 :

Error Position	Binary value of error position				
0 (no error)	p5	p4	p3	p2	p1
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0
21	1	0	1	0	1

5

Figure 6: Figure 5 :



6

Figure 7: Figure 6 :

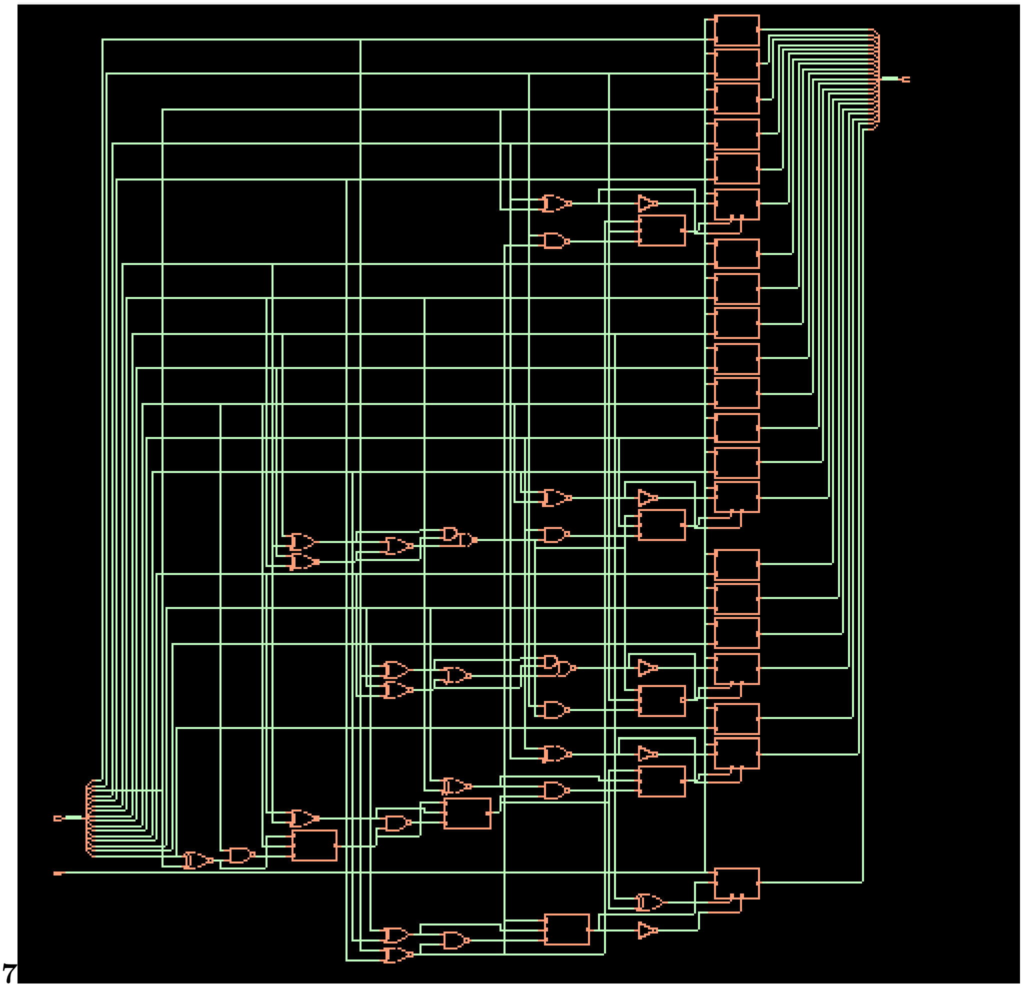
7


Figure 8: Figure 7 :

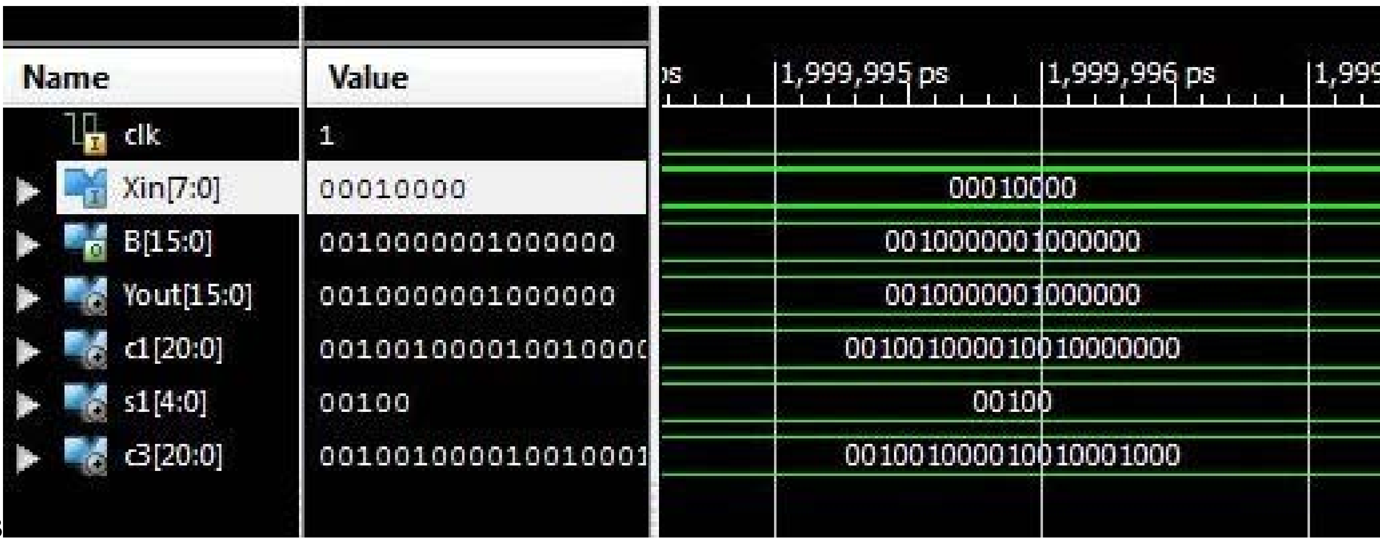
8


Figure 9: Figure 8 :

[Reviriego et al. (2012)] 'Area efficient concurrent error detection and correction for parallel filters'. P Reviriego , S Pontarelli , C Bleakley , J A Maestro . *IET Electron. Lett* Sep. 2012. 48 (20) p. .

[Oppenheim and Schafer ()] *Discrete Time Signal Processing*, A V Oppenheim , R W Schafer . 1999. Upper Saddle River, NJ, USA: Prentice-Hall.

[Hamming (1950)] 'Error correcting and error detecting codes'. R W Hamming . *Bell Syst. Tech. J* Apr. 1950. 29 p. .

[Sneha and Jamuna (2015)] 'FPGA Implementation of Reduced Precision Redundancy Protected Parallel Fir Filters'. P Sneha , S Jamuna . *IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)* May -Jun.2015. Ver. II. 10 (3) p. .

[Gao et al. ()] Zhen Gao , Pedro Reviriego , Wen Pan , Zhan Xu , Ming Zhao , Jing Wang , Juan Antonio Maestro . *Fault Tolerant Parallel Filters Based on Error Correction Codes*, 2014. IEEE. p. .

[Lin and Costello ()] S Lin , D J Costello . *Error Control Coding*, (NJ, USA) 2004. Prentice-Hall. (2nd ed. Englewood Cliffs)

[Single Error Correction and Double Error Detection (SECDED) with CoolRunner-II? CPLDs Xilinx, XAPP383 (v1.1) (2003)] 'Single Error Correction and Double Error Detection (SECDED) with CoolRunner-II? CPLDs'. *Xilinx, XAPP383 (v1.1)*, August 1, 2003.

[Daitx et al. ()] 'VHDL Generation of Optimized FIR Filters'. F Daitx , S R Vagner , Eduardo Costa , Paulo Flores , S Bampi . *IEEE International Conference on Signals, Circuits and Systems*, 2008.