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Reduction of Power Consumption using Different Coding Schemes using FPGA in NoC

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Abstract

Network-On-Chip (NoC) is used as a main part of a system. NoC overcomes traditional System-On-Chip (SoC) problems. Because, SoC has problems like cost, design risk, more complexity and more power consumption. In software part, Xilinx ISE Design suite 14.5 with VHDL programming is used. It is simple programming language. In hardware part, FPGA of Spartan 3E family is used. It is advanced 90nm technology. It is world?s the cheapest FPGA family. It has 500K gates and 40 LUTs. It has lowest cost per logic. Its better advantage is that it is designed for more volume-to-market. Power consumption of given system is compared with previous system. From output power analysis chart, it is concluded that given system has lower power consumption than previous system. Power consumption of gray to binary conversion block of previous system is nearly equal to power consumption of present (given) whole system. This proves that there is a great reduction in power consumption in the system.

Index terms— FPGA, LUTs, Network-on-Chip (NoC), System-on-Chip (SoC), Spartan 3E, VHDL.

1 I. Introduction

Design density and total length of interconnection wires are directly proportional with each other. This affects on long distant transmission delay and higher power consumption.

2 II. Related Work

Giuseppe Ascia, et al. [1],

In this paper, we propose the data encoding techniques are used to reduce both power dissipation and energy consumption of NoC links Working on the basis of end-to-end, the proposed encoding scheme exploits the wormhole switching techniques.

That is, encoding and decoding of flits by NIs at source and destination. Shivaraj MN, et al. [2], Jeeva Anusha,et al. [3],

In the proposed system, different encoding schemes are given. Also, hardware design properties are presented. Output details and power details are given.

3 III. Proposed System

In method 1, Encoding is done by reducing number of type-I, II transitions and converting them to type-III and / or Type IV transition. Network-on-Chip power dissipation sources (links) [1] s process technology scaling continues number of transistor increases and hence power consumption also increases. Chip-multiprocessor can reach higher efficiency due to synchronized parallel execution of multiple programs or threads. Network-on-Chip is a scalable alternative to conventional when core count is more in Chip-multiprocessor. For mainly in current VLSI design, power efficiency is very important constraint in NoC design. In this paper, encoding techniques

are used to reduce dynamic power reduction than previous system. Coupling switching activities are reduced. Detailed process of inversion is explained with the help of flowchart.

Author ? ?: Electronics and telecommunication, Department Bharati Vidyapeeth's College of Engineering for Women Pune, 43 , Savitribai Phule Pune University, Maharashtra, India. e-mails: suvarna.chorage@bharatividyapeeth.edu, snehamitkari@gmail.com Here, capacitance is in µF. So, it is very negligible.

() (3)**2**

From (2) and (4),

From (2) and (**??**),

We know energy formula with respect to voltage and capacitance.

These two formulae are the basic formulae for energy and power. ? As shown in Table **??**2, number of logics increases efficiency. As number of signals decreases power consumption also decreases from scheme-1to scheme-3. ? In previous system, for only one stage, i.e. Gray Encoding block, dynamic power consumption was 0.3mW.And now, in the present system after summing for all stages, dynamic power consumption is 0.46mW.From this comparison is done. We can conclude that power consumption is minimized in more amounts.W = (1/2)(???? 2) P = W/t W = VIt W/t = VIt /t = VI P = VI W/t = (1/2)(???? 2)/t 1/2 (???? 2)f = P P = (1/2)(?????? 2)

4 VI. Results and Discussion

a) Scheme-I In scheme-I, half invert and full invert is performed. In full invert, 00 is converted into 11. When any one of the two is performed then inversion bit is set to 1, otherwise it is set to 0.

5 b) Scheme-II

Simulation is done on Xilinx 14.5 ISE simulator. It is backend design tool. In scheme-II odd inversion is added. Type-II transitions are converted into type-IV transitions. Data coming at Network interface is from Encoder block. Then it is converted into desired encoded data which is passed through number of routers. This type of encoding is of scheme-II.

6 c) Scheme-III

In scheme-III, there is additional inversion is performed that is Even inversion. For that Te block is added in second stage. Here, power consumption will be less than Scheme-II because; link power consumption is minimized in more amounts.

Binary bit has some switching problem. So, they are converted into gray bits.

7 d) Results obtained by LCD Interfacing

To calculate report for power consumption, first, we have to interface encoder and decoder with LCD. On this LCD, we can see desired output for both stages, encoding and decoding.

Here, 'en' is for enable, 'clk' is for clock and 'rs' is for register select. When there is initialization of lcd rs=0. When rs=1, data is as it is written on lcd. When en=1, module is enabled or is started.

8 VII. Conclusion

? Encoding and decoding operation is used for security purpose. But here, main aim is to reduce power consumption in a effective way. ? Hardware part is used in such a way that cost of Spartan 3E (for Xilinx) is the lowest among different FPGA families. ? Dynamic power consumption without interfacing is calculated and compared with previous systems. ? In scheme-I, II, III, on the basis of parameters, power analysis is done.

9 A

Reduction of Power Consumption using Different Coding Schemes using FPGA in NoC [1] [2]

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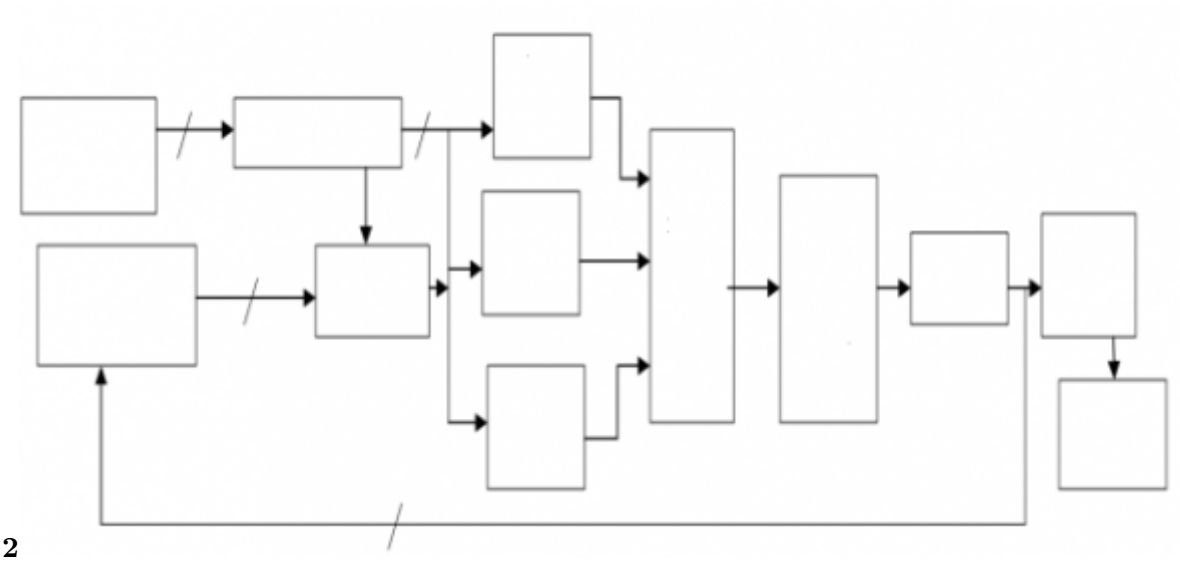


2

Figure 1: Fig. 2 :

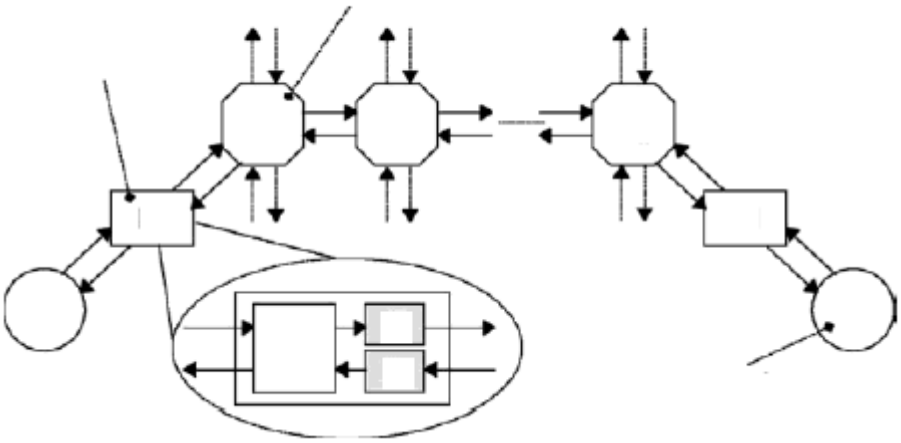
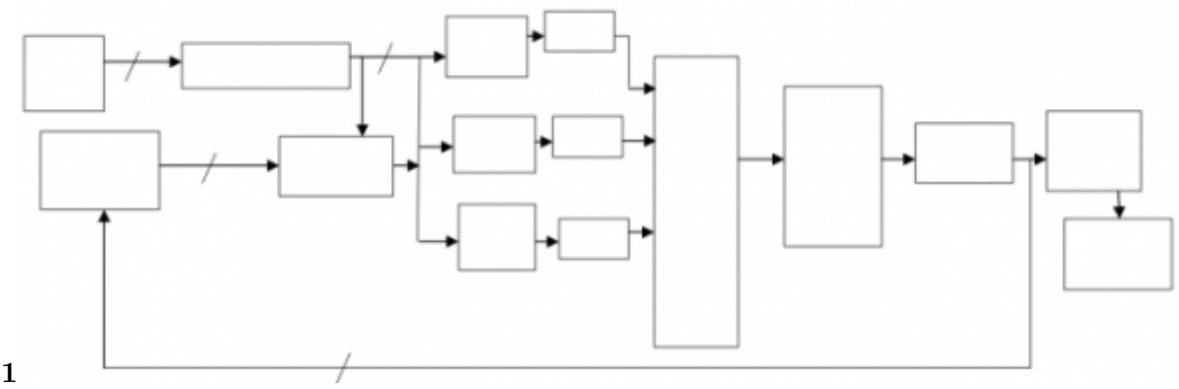


Figure 2: A



1

Figure 3: Fig. 1 :

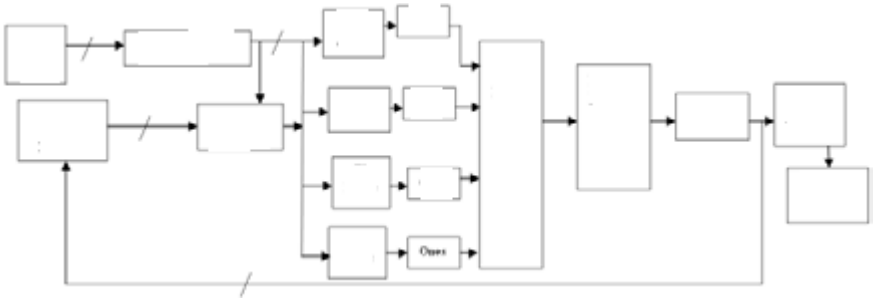


Figure 4:

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Figure 5: Fig. 5 :

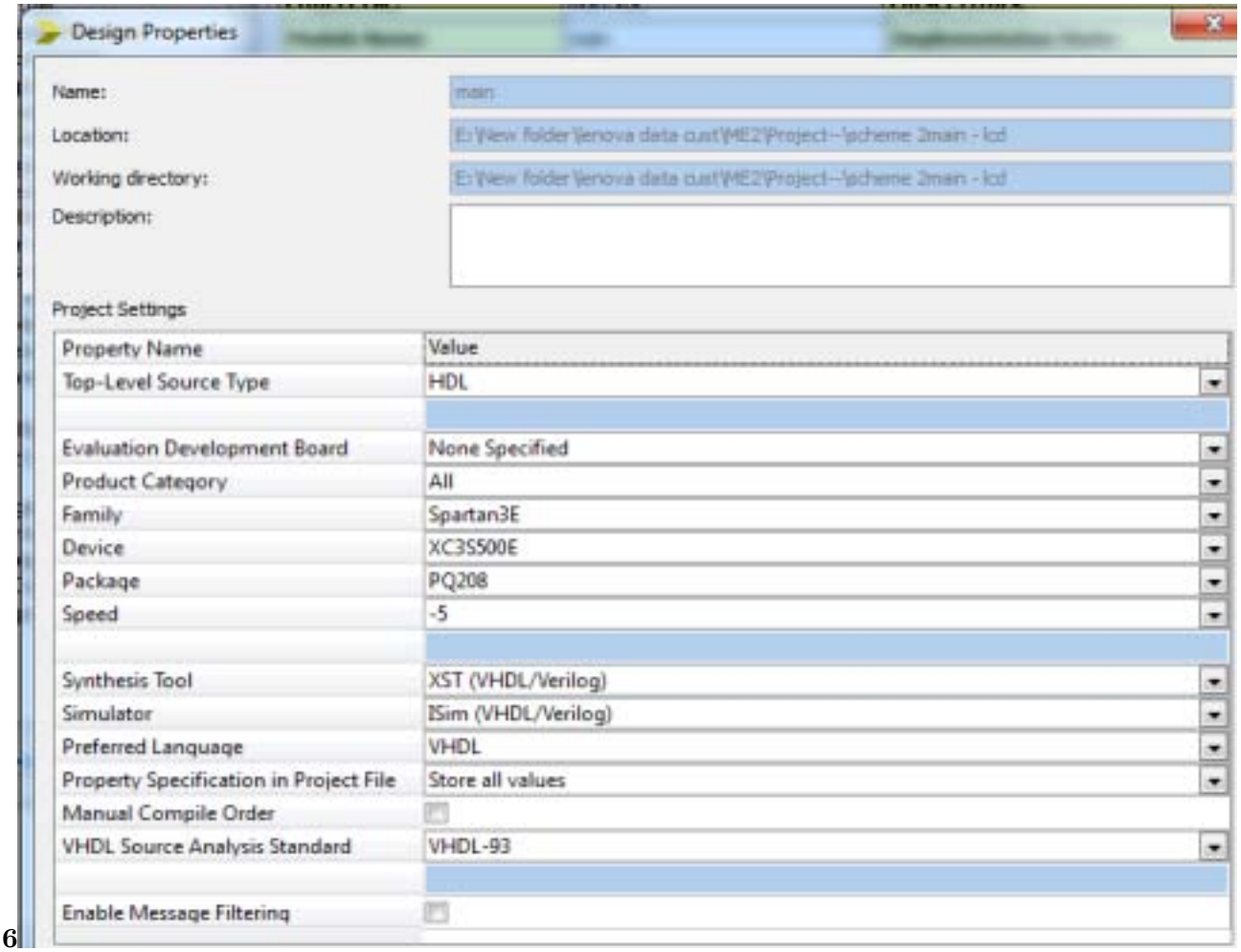

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Figure 6: Fig. 6 :

On-Chip	Power (mW)	Used	Available	Utilization (%)
Clocks	0.46	1	---	---
Logic	0.00	144	5720	3
Signals	0.00	175	---	---
IOs	0.00	20	102	20
Static Power	13.69			
Total	14.15			

2.2. Thermal Summary

Thermal Summary	
Effective TJA (C/W)	38.4
Max Ambient (C)	84.5
Junction Temp (C)	25.5

2.3. Power Supply Summary

Power Supply Summary			
	Total	Dynamic	Static Power
Supply Power (mW)	14.15	0.46	13.69

Figure 7: Fig. 3 :Fig. 4 :Fig. 4 :

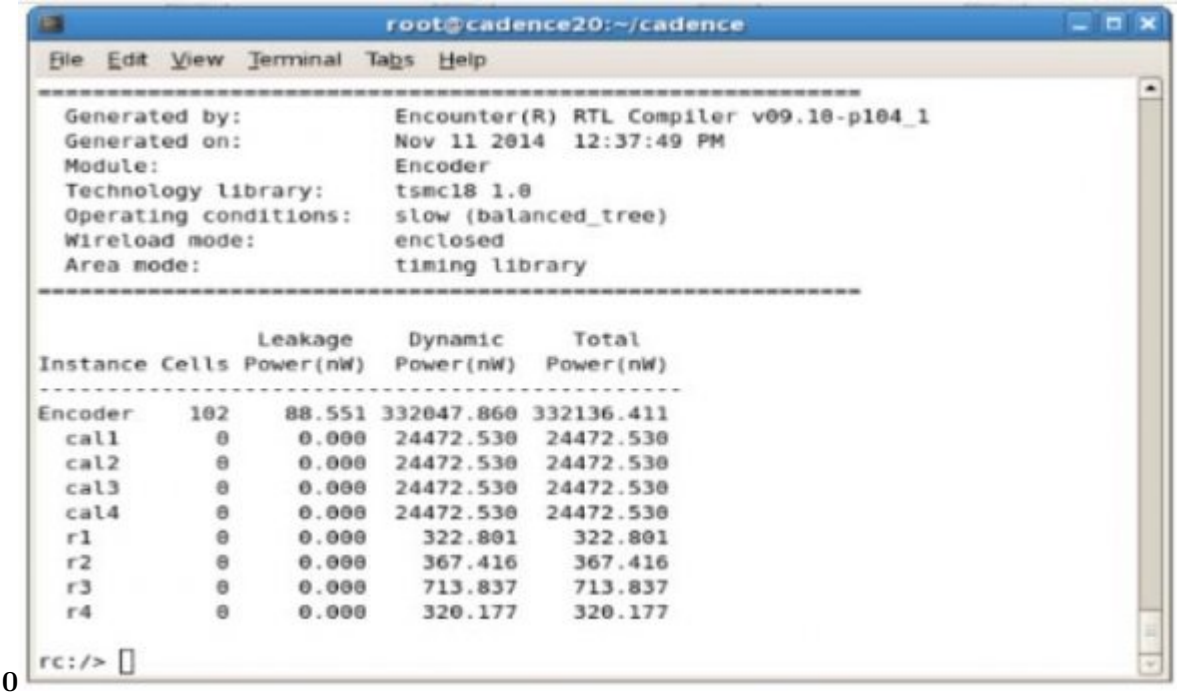

Figure 8: A 4]Fig. 7 :Fig. 8 :Fig. 9 :Fig. 10 :

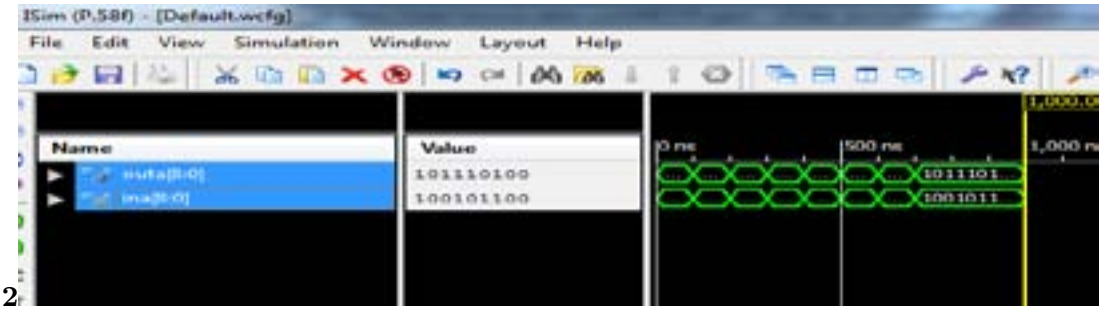

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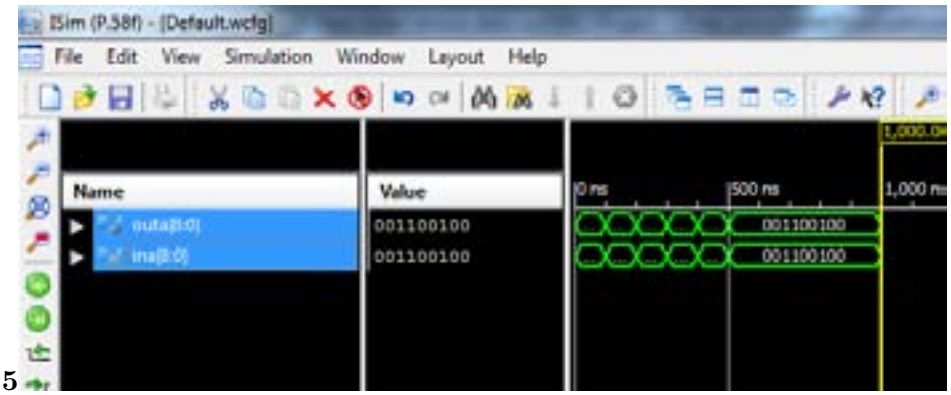
Figure 9: Fig. 12 :



15

Figure 10: Fig. 15 :

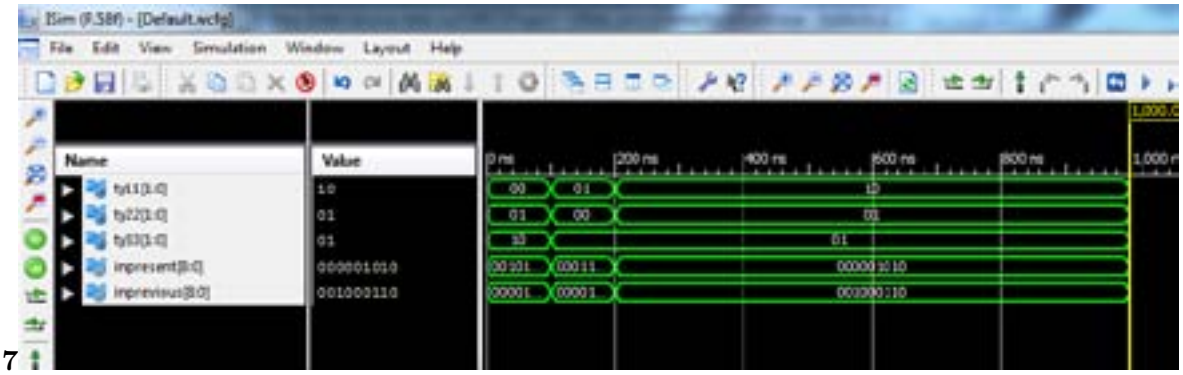


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Figure 11: Fig. 17 :

2

Parameter	Scheme-1	Scheme-2	Scheme-3
Family	Spartan-3E	Spartan-3E	Spartan-3E
Device	XC3S500E XC3S500E XC3S500E		
Package	PQ208	PQ208	PQ208
Speed	5	5	5
Clock	1	1	1
Logics	148	163	144
Signals	197	177	175
IOs	20	11	20
Dynamic Power	0.46mW	0.46mW	0.46mW
Static Power	13.69mW	13.69mW	13.69mW

Figure 12: Table 2 :

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