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Using Neural Networks to Design Transistor Amplifier Circuits

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Abstract- This paper is an extension of previous work that addressed the application of bipolar transistor amplifier design using neural networks. That work addressed the design of common emitter amplifiers by first mathematically determining specific output parameters from a large selection of biasing resistors. Once the outputs had been determined, a neural network was trained, using the aforementioned results as inputs and the biasing resistors as outputs. This was initially performed with ideal emitter bypass capacitors, but was then followed-up by employing several non-ideal capacitors, making it much more interesting and useful. This paper focuses on the common collector and the common base configurations. Bipolar junction transistor amplifier parameters often include voltage gain, input impedance, output impedance, and the voltage difference between the collector and emitter. These will be addressed in this paper as before.

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Using Neural Networks to Design Transistor Amplifier Circuits

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Abstract- This paper is an extension of previous work that addressed the application of bipolar transistor amplifier design using neural networks. That work addressed the design of common emitter amplifiers by first mathematically determining specific output parameters from a large selection of biasing resistors. Once the outputs had been determined, a neural network was trained, using the aforementioned results as inputs and the biasing resistors as outputs. This was initially performed with ideal emitter bypass capacitors, but was then followed-up by employing several non-ideal capacitors, making it much more interesting and useful. This paper focuses on the common collector and the common base configurations. Bipolar junction transistor amplifier parameters often include voltage gain, input impedance, output impedance, and the voltage difference between the collector and emitter. These will be addressed in this paper as before. There are several methods that can provide a suitable solution for each design, however the objective of this work is to indicate which external resistors are necessary to yield useful results by employing neural networks.

Keywords: feedforward neural networks, bipolar junction transistor circuits, common collector amplifier, common base amplifier.

I. Introduction

This paper addresses two amplifier topologies that use bipolar junction transistors (BJTs). In a previous paper a common emitter amplifier was evaluated and it was determined that the value of the bypass capacitor played a significant role in the voltage gain and other parameters due to the low emitter resistance of the transistor [1]. It was also established through simulations and analysis that the coupling capacitors did not affect the results of required amplifier parameters to any great extent. Here we address the common collector amplifier, otherwise known as the emitter follower, and the common base amplifier. Both configurations employ coupling capacitors, so for this work they will be considered as ideal. The output impedance of the source and the input impedance of the load can be factored in after developing the initial model.

For either amplifier design, and for a given transistor, the designer works through a set of calculations to determine the biasing resistor values, then often has to modify those values to achieve the proper voltage gain (A_v), input impedance (R_{in}), output impedance (R_o), and voltage difference between the collector and emitter (V_{ce}). This latter parameter can affect whether the amplifier enters saturation or cutoff. For the common collector amplifier the voltage gain is just under unity, as shown later.

The goal of this work is primarily intended for engineers, but others may want to evaluate specific amplifier designs based on the results illustrated in this paper. For any specific amplifier design, the neural network should be able to provide reasonably close biasing resistor values, provided that the parameters input by the user are within appropriate limits. It is hoped that with the addition of these two amplifier designs to the common emitter circuit shown in a previous paper, the user will be able to approximate the appropriate resistor values in a streamlined manner.

This paper is organized as follows. First, the design procedure for the dc equivalent common collector circuit is introduced along with some of its defining equations. Next, the expressions needed to solve for the ac equivalent circuit are developed. This is followed by a brief discussion of the neural network architecture and results. The next section addresses the common base ac equivalent circuit and the corresponding results. Finally, some conclusions will be discussed and some thoughts for further work. When analyzing both of these amplifiers there are the dc bias values and the ac signals to contend with, but one must look at each of them separately in order to compute the proper operating points.

II. The Common Collector Amplifier

The common collector circuit is one of the basic configurations introduced when studying the BJT [2]-[4]. It is considered as a voltage buffer providing a high input impedance and a low output impedance, which is useful for impedance matching with other circuits. As stated above, the voltage gain of this circuit is approximately equal to one.An example of the common collector amplifier is shown in Fig. 1 where the 2N3904 NPN transistor is used with β=160. The ac input is Vi while the output is taken from the emitter terminal.For this amplifier the neural network is designed to accept three input parameters: input resistance (R_{in}), output resistance (R_{out}), and the voltage across the collector-emitter junction (V_{ce}). The objective of the network is to provide the biasing resistors R_{b1}, R_{b2}, and R_e, needed to achieve the desired results.

Initially, the dc circuit is analyzed with all capacitors considered as open circuits in order to find

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the currents and voltages from the power supply and biasing resistors. The coupling capacitors isolate the dc component where its circuit equivalent is shown in Fig. 2.As in the previous work, the dc biasing voltage was 15 volts for both circuits described in this paper. All input signals were set to 3 kHz sinusoids.

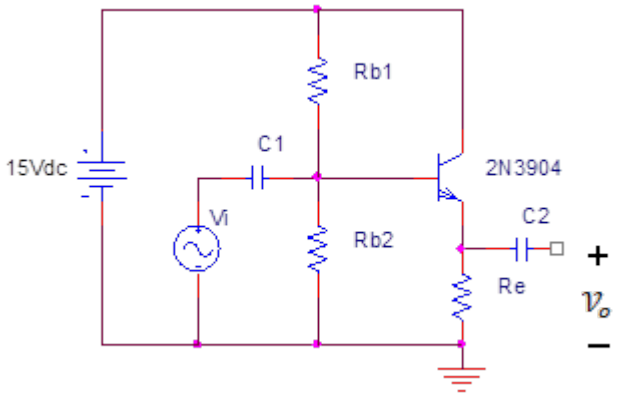

Fig. 1: Common collector amplifier circuit.

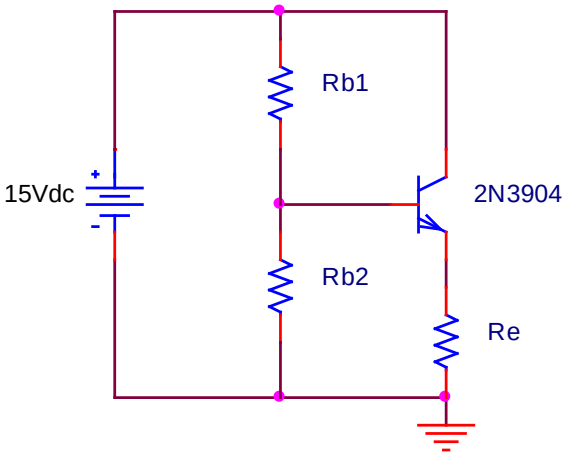

Fig. 2: The dc equivalent circuit of a common collector amplifier.

To determine the dc biasing values, the base resistors and source are replaced with their Thevenin equivalents as shown here.

$$V_{th} = V_{cc}\left(\frac{R_{b2}}{R_{b1}+R_{b2}}\right) \quad \text{and} \quad R_b = R_{b1}||R_{b2} \tag{1}$$

This allows a single loop circuit to be analyzed as in (2) where the base current, I_B, can be determined.

$$-V_{th} + R_b\, I_B + 0.7 + (\beta + 1) I_B R_e = 0 \tag{2}$$

After the dc bias values have been found those sources are set to zero and only the ac components are considered. Recall that the dc voltage sources become short circuits to ground when set to zero. The ac equivalent of the transistor circuit is shown in Fig. 3 using the hybrid – π model [4]. The ac values of input and output resistance, along with V_{ce} are computed from the dc bias currents.

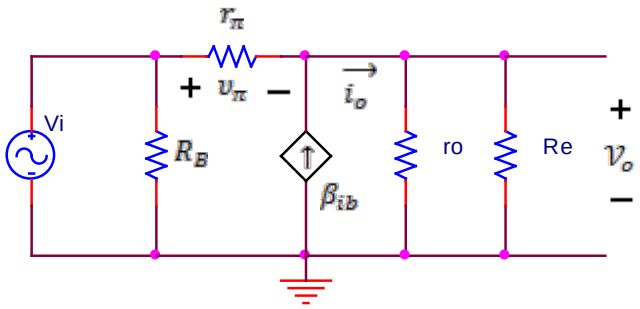

Fig. 3: The ac equivalent circuit of the common collector amplifier.

Most of the ac equivalent expressions can be found in texts on microelectronics so they are only summarized here. As shown below, the total collector current i_C is ascertained where v_{be} is the ac base to emitter voltage and V_T is the thermal voltage, usually approximated at 25 mV yielding:

$$i_C \approx I_C\left[1 + \frac{v_{be}}{V_T}\right] = I_C + \left(\frac{I_C}{V_T}\right) v_{be} \tag{3}$$

From now on the ac component is of interest and the DC sources are shut down. By looking at the far right term from equation 3 it can be seen that the ac equivalent is:

$$i_c = \left(\frac{I_C}{V_T}\right) v_{be} \tag{4}$$

The component in parenthesis is referred to as the transconductance, with symbol g_m so:

$$g_m = I_C / V_T \tag{5}$$

therefore:

$$i_c = g_m\, v_{be} \tag{6}$$

The ac input resistance of the transistor itself is given as

$$r_\pi = v_{be}/i_b = v_{be}/(g_m\, v_{be}/\beta) = \beta/g_m \tag{7}$$

Or alternatively

$$r_\pi = \beta/(I_C/V_T) = \beta/(\beta\, I_B/V_T) = V_T/I_B \tag{8}$$

Note from Fig. 3 that:

$$i_o = (\beta + 1) i_b \tag{9}$$

So the output voltage can be computed as:

$$v_o = i_b(\beta + 1)(r_o||R_E) \tag{10}$$

where r_o is the resistance seen looking into the collector and is often calculated as $100/I_C$.

By writing a KVL equation around the base-emitter loop we arrive at:

$$v_{in} = i_b[r_\pi + (\beta + 1)(r_o||R_E)] \quad (11)$$

The small signal input impedance results from dividing the expression above by the base current yielding:

$$R_{ib} = \frac{v_{in}}{i_b} = r_\pi + (\beta + 1)(r_o||R_E) \quad (12)$$

Taking into account the two biasing resistors R_{b1} andR_{b2} which are in parallel withR_{ib} the overall input impedance of the amplifier is:

$$R_{in} = R_{b1}||R_{b2}||R_{ib} \quad (13)$$

As one might expect, the input impedance of this amplifier is significant, resulting in a very low loading effect on stages that might precede it. By combining equations (10) and (12) the voltage gain is determined to be:

$$A_v = \frac{(\beta+1)(r_o||R_E)}{r_\pi+(\beta+1)(r_o||R_E)} \approx 1 \quad (14)$$

Computing the output impedance,R_o, is somewhat involved, so only the result will be presented here where it can be seen as being very low due to the $\beta + 1$ factor. It can be on the order of tens of ohms.

$$R_o = \frac{r_\pi}{\beta+1}||R_E||r_o \quad (15)$$

III. Neural Networks

Neural networks are most commonly considered as pattern recognition systems. This author has used them to develop a method of impedance matching using feed-forward neural networks [5] and also in the design of common emitter amplifiers [1]. They are non-linear systems and are often employed to separate input patterns by setting up a set of hyperplanes in n-dimensional space [6] - [8].

In order to train the neural networks in this project a set of "for" loops was created in MATLAB®for the three biasing resistors. For all of the tests, the resistor values ranged as shown in table I. Since the voltage gain is near unity for the common collector amplifier it was not addressed in this work.

Table 1: Resistor values used to Develop Output Parameters

Resistor	Start value	Step Value	Stop Value
Rb1	4 kΩ	250 Ω	10 kΩ
Rb2	4 kΩ	250 Ω	10 kΩ
Re	400 Ω	100 Ω	1.5 kΩ

The values of R_{in}, R_o, and V_{ce} were calculated for all of the resistor combinations. Once this was completed a neural network was trained using the new input values of the three parameters above to compute the three biasing resistor values. In developing the network, the inputs and outputs were normalized to ensure convergence. For this circuit there were 7,500 training patterns, limited to realistic output values. For example, V_{ce} was held to the range of 2 volts to 12 volts. The test sets consisted of a larger number of patterns, none of which had been used in training.

The neural network package in MATLAB® was employed to train the networks, by utilizing the Levenberg-Marquardt algorithm, using one hidden layer of 14 sigmoidal (Tanh) neurons each [9]. As noted in the previous work, a lesser number of nodes yielded unacceptable results, and more nodes or more than one hidden layer did not provide any improvement in performance. The network was trained for 2000 epochs resulting in a mean-squared error (mse) of $2.45x10^{-8}$. Further training did not seem improve performance. A comparison between the neural network results and those by direct calculation is shown in table II. Fig. 4 shows the architecture of the neural network. This network employs hyperbolic tangent activation functions to map the transistor parameters to the values of the resistors.

Table 2: Statistical performance of neural network

Data type	Number of patterns	Upper base resistor Rb1(mse)	Lower base resistor Rb2(mse)	Emitter resistor Re(mse)
Training set	7500	0.784	6.00	0.0131
Test Set #1	8316	1.48	7.80	0.0225
Test Set #2	10440	1.39	7.20	0.020
Test Set #3	11160	1.23	6.71	0.018
Test Set #4	13728	1.41	7.24	0.020

The training set was included for comparative purposes.

The number of patterns changes with all of the training and testing scenarios because as the values of the biasing resistors change, the outputs can fall out of the ranges specified earlier. Only those that fall within those ranges are employed in the tests. When using the resistance values illustrated in table I the output parameters have the ranges shown in table III. It is not required that these ranges be followed precisely but it is likely a good practice to stay within them when considering an input set.

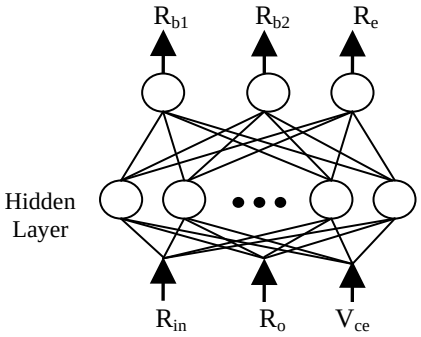

Fig.4: Architecture of the neural network with 14 hidden nodes.

Table 3: Input parameter ranges

Parameter	Minimum value	Maximum Value
Rin	1.94 k Ω	4.90 kΩ
Ro	1.4 Ω	10.5Ω
Vce	5.1 V	11.6 v

It is important to realize that not all input parameter combinations are feasible. For example, if the base bias resistors are kept to a low value the collector and emitter currents can be greater, resulting in a smaller value of V_{ce}. In this case it would not be appropriate to set a small value of dc input resistance and a large value of V_{ce}, since they can be mutually exclusive. However, by judiciously choosing realistic inputs the results can be close to the desired values. Some comparisons of the neural network out against calculation are shown in table IV. During the testing phase the network was asked to determine the resistor values for three different ac parameters. The input impedances, output impedances, V_{ce}, and the values of the resistors predicted by the network were recorded. The resistor values from the network were then used to calculate those same ac values directly. The results were remarkably good as shown in table IV.

Table 4: Expectedac parameters and the associated percent errorsagainst the neural nework output

Rin (Ω)	%error	Ro (Ω)	% error	Vce	%error
2402	0.083	2.634	0.076	6.67	0.075
3101	0.032	3.386	0.003	5.695	0.004
4310	0.001	3.583	0.002	7.547	0.013

The resistor values from the last trial from table IV were used in a P-Spice simulation. The values were $R_{b1} = 7.96k\Omega$, $R_{b2} = 9.98k\,\Omega$ and $R_e = 1.07k\,\Omega$. The results are summarized in table V along with the percent errors.

Table 5: Comparison of neural network results against the P-Spice simulation

Parameters	Neural Network	P-Spice	% difference
Rin	4310Ω	4274Ω	-0.835
Ro	3.583Ω	3.546Ω	-1.033
Vce	7.547V	7.549V	0.027

IV. The Common Base Amplifier

The second circuit addressed in this paper is the common base amplifier. The hybrid – π model of the transistor is also used. The DC analysis of this circuit is essentially the same as for the previous one except that it has collector resistor, so it will not be addressed here. The ac equivalent of a common base amplifier is shown in Fig. 5 in which the base is at signal ground. The input is at the emitter and the output is at the collector. A summary of the voltage gain, current gain, input impedance, and output impedance is presented here. As in the other configurations, the output impedance of the signal source is not included, since that parameter would be unknown for the individual amplifiers.

$$A_v = g_m R_C \tag{16}$$

The current gain can be approximated by:

$$A_i \approx \frac{\beta}{\beta+1} = \alpha < 1 \tag{17}$$

The input resistance of the amplifier R_{ie} is quite low where the input signal sees the emitter resistance r_e:

$$R_{ie} = \frac{r_\pi}{\beta+1} = r_e \tag{18}$$

The output resistance R_o is approximated as:

$$R_o = r_o || R_C \tag{19}$$

One may wonder about the significance of this circuit but since the output impedance looking back into the collector is very large. However due to this characteristic it behaves almost like an ideal current source. It is sometimes referred to as a current buffer.

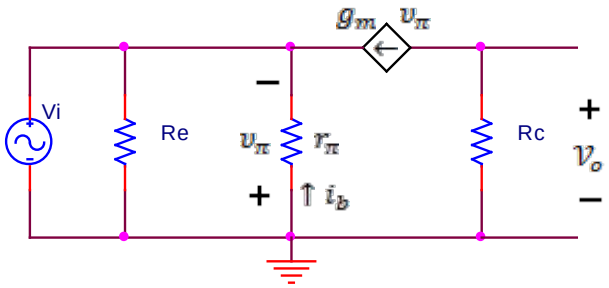

Fig. 5: This is the ac equivalent circuit of the common base amplifier.

Table VI lists the biasing resistors used in the common base configuration.

Table 6: Resistor values used to develop output parameters

Resistor	Start value	Step Value	Stop Value
Rb1	4 kΩ	250 Ω	10 kΩ
Rb2	4 kΩ	250 Ω	10 kΩ
Rc	1 kΩ	100 Ω	3 kΩ
Re	400 Ω	100 Ω	1.5 kΩ

As in the common collector circuit, the values of Rin, Ro, and Vce were calculated for all of the resistor combinations. Again, V_{ce} was held to a range of 2 volts to 12 volts.

Here the network consisted of one hidden layer of 14 sigmoidal neurons. The network was trained for 1904 epochs resulting in a msetargetof$1.0x10^{-8}$. A comparison of the results obtained from the network against the true values of resistance are revealed in table VII for several different test sets.

Table 7: Resistor values used to develop output parameters

Data type	Number of patterns	Upper base resistor Rb1(mse)	Lower base resistor Rb2(mse)	Collector resistor Rc(mse)	Emitter resistor Re(mse)
Training set	5676	0.704	1.24	0.031	0.038
Test Set #1	6242	0.656	1.20	0.030	0.035
Test Set #2	8108	0.603	1.10	0.027	0.031
Test Set #3	9135	0.560	1.10	0.281	0.030
Test Set #4	10938	0..627	1.11	0.029	0.323

The training set was included for comparative purposes.

The number of patterns changes with all of the training and testing scenarios because as the values of the biasing resistors change, the can fall out of the ranges specified earlier. Only those that fall within those ranges were employed in the tests. When using the resistance values illustrated in table VI the output parameters have the ranges shown in table VIII. It is not required that these ranges be followed precisely but it is likely a good practice to stay within them when considering an input

Table 8: Input parameter ranges

Parameter	Minimum value	Maximum Value
Ro	950 Ω	2.092 kΩ
Av	93.9 V/V	210 V/V
Vce	2.02 V	9.11 V

For the common base amplifier the voltage gain was the primary focus, however the output impedance and V_{ce} were also determined. The input impedance was more problematic. For this amplifier, several combinations of resistor values yielded the same input impedance values. Therefore, when training from the input impedance to find the bias resistors, the network experienced multiple targets meaning that the network could not converge. Several experiments that included input impedance were conducted, but the results were unsuccessful. For this amplifier the input impedance is very low, and from the bias resistors contained in table VI, Rin only ranged from about 4.7Ω to 10.6Ω. In this case it might be prudent to approximate the value as 7.5Ω for most applications. The results between the neural network and those by direct calculation are shown in table IX.

Table 9: Expected AC parameters and the associated percent errorsagainst the neural nework output

Ro (kΩ)	% error	Av V/V	% error	Vce	% error
1.305	0.19	206	2.12	4.17	0.84
1.748	-0.34	202	1.03	5.78	-0.76
1.045	0.012	207	2.51	3.24V	0.24

The resistor values from the last trial from table IX were used in a P-Spice simulation with $R_{b1} = 9\ k\Omega, R_{b2} = 4.5k\Omega$, $R_C = 1.1k\Omega$, and $R_E = 600\Omega$. The results are summarized in table X along with the percent errors.

Table 10: Comparison of neural network results against the P-Spice simulation

Parameters	Neural Network	P-Spice	% difference
Ro	1.045kΩ	1.05kΩ	0.478
Av	207V/V	211V/V	1.93
Vce	3.24V	3.27V	0.926

V. Conclusions and Further Work

It was remarkable how well the network results compared against those from direct calculation and from P-Spice. Several experiments were conducted more than once, and the output values checked frequently, to be certain there were no errors.

This has been an interesting research project as a follow-up to previous work. Here, two classical BJT amplifiers have been analyzed, then synthesized by a set of neural networks. In both cases the capacitors did not play a significant role and were considered to be ideal. This neural network paradigm should be useful to engineers and faculty members when looking for solutions to various designs. The research described in this paper can help to resolve and verify transistor solutions for both configurations and can illustrate the efficacy of neural networks as a tool for this branch of amplifier design. It is the intension of this author to look into other, more complex amplifier designs, such as the cascode circuit which is a multistage system, consisting of a common emitter amplifier driving a common base amplifier.

References Références Referencias

1. Hemminger, T. L., "A Neural Network Approach to Transistor Circuit Design", Global Journal of Computer Science and Technology, Vol.16, Issue 1, Version 1.0, 2016.
2. Sedra, A.S., and Smith, K.C., *"Microelectronic Circuits,"* Oxford University Press, Seventh Ed., 2015, chapter 7.
3. Jaeger, R.C., *"Microelectronic Circuit Design,"* McGraw-Hill, 1997, chapter 13.
4. Neamen, D.A., *"Microelectronics Circuit Analysis and Design,"* McGraw-Hill, 2010, chapter 6.
5. Hemminger, T. L., "Understanding Transmission Line Impedance Matching using Neural Networks and PowerPoint," Frontiers in Education, 2005, T4E.
6. Pao, Y, H., Adaptive Pattern Recognition and Neural Networks, Addison-Wesley, 1989.
7. Graupe, D., "Principles of Artificial Neural Networks" World Scientific, 2013.
8. Hagan, M. T., Demuth, H, B. "Neural Network Design", Second Ed.
9. Demuth, H. T., Beale, M., "Neural Network Toolbox," The Mathworks Inc.