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FPGA Implementation of NPSF Testing using Block Code Technique

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Abstract

This paper presents a test structure for high speed memories. Built in self test (BIST) give the solution for testing memories and associate hardware for test pattern generation and application for a variety of test algorithms. Memory test algorithm for neighborhood pattern sensitive faults (NPSF) is developed by using block code technique to identify the base cell and deleted neighborhood cells. Test pattern generation can be done by using LFSR and Euler pattern generation. The testing process is verified using Xilinx ISE 14.2 and implemented on Nexys 4 DDR Artix 7 FPGA board.

Index terms— LFSR pattern generation, euler pattern generation, block code technique, Nexys 4 DDR Artix 7 FPGA.

1 Introduction

uilt in self test (BIST) design technique is a part of circuit which is used to test the circuit itself. Engineers design BISTs to satisfy demands such as lower repair cycle times or constraints such as limited technician accessibility and cost of testing during manufacture and high reliability. The main purpose of BIST is to reduce the test complexity, and thereby decrease the cost and reduce dependence upon external (pattern programmed) test equipment [1]. Built in self test techniques are very useful in testing of logic circuits, because they offer a cost effective way to test complex digital devices. First the BIST concept was implemented on combinational circuits, after that it found quick demands in the testing of regular structures like programmable logic arrays, read only memories, and random access memories.

Quick increment of multifaceted nature in the integrated circuits has prompt impact following on memory testing. On one view, the limit of randomaccess memories upgrades, in this manner expanding the test time and cost, on the other view, the complexity of memory circuits becomes more, and therefore more failure modes and faults should be considered in order to get a product with good quality [4]. Accordingly, different constraints need to take care while considering a test algorithm.

Minimizing the number of memory operations in order to allow large capacity memories to be tested in proper period of time and covering a larger collection of memory faults. In the last previous days of memory design test procedures were developed in an ad-hoc manner. The fault coverage of these ad-hoc test procedures was limited and often indeterminable [2]. This shortcoming, acknowledged by most researchers, motivated the introduction of such fault models as stuck-at faults, decoder faults, coupling faults. If density of memory circuits increases, it increases coupling effects then the pattern sensitive fault PSF is becoming very important fault model [3].

The

2 b) Neighborhoods Pattern Sensitive Faults

A Pattern Sensitive Fault is a restrictive coupling fault in which the content of a memory cell, or the capacity to change its content, is affected by a specific bit pattern in different cells in the memory. Here the information maintenance and change of the victim cell are influenced by an arrangement of aggressor cells. A neighborhood pattern sensitive Fault (NPSF) is a special instance of pattern sensitive faults [8], wherein the affecting (coupling) cells are in the neighborhood of the impacted (coupled) cell. The coupled cell is known as the base (or victim) cell and the coupling cells are known as the deleted neighborhood cells. The neighborhood incorporates 4 deleted

neighborhoods and one base cell. It forms the coupling of these 4 cells with the base cell considering effect as the NPSF fault modeling.

3 c) Active NPSF

The base cell changes its contents because of changes in the deleted neighborhood pattern. To identify these affect, every cell must be read in state 0 and in state 1 for every single conceivable change in the deleted neighborhood pattern. There are two distinctive conceivable states for the base cell (0 and 1), N-1 methods for picking the deleted neighborhood cell which must experience one of two conceivable advances (? or â??"), and N-2 potential outcomes for the rest of the neighborhood cell contents.

2* (N-1)*2*2N-2 = (N-1)* 2N is the aggregate number [8] of active neighborhood patterns (ANPs). It require 128 patterns for identifying active NPSF faults. For type-1 NPSF, 2 is base cell and 0, 1, 3 and 4 are deleted neighborhood cells.

4 d) Passive NPSF

The content of the base cell can't be changed because of a specific neighborhood pattern. Every cell must be written and read in state 0 and in state 1 for all changes of the deleted neighborhood pattern. For each of the 2N-1 deleted neighborhood patterns, the two conceivable advances ? and â??" must be confirmed. Subsequently, the aggregate number of PNPSFs is 2*2N-1=2N. Here N is number of cells. It require 32 test patterns for recognizing active NPSF faults.

5 e) Static NPSF

The content of a base cell is compelled to a specific state because of a specific neighborhood pattern. To distinguish these faults, apply the 2N combinations of 0s and 1s to the N-cell neighborhood, and check by perusing every cell that each pattern can be stored. It varies from ANPSF that it is not necessary to have a change to transition to sensitize an SNPSF. We required 32 test patterns for recognizing static NPSF faults. Fig **??** shows that the memory is divided into nine different blocks. Nine test cases are used for testing the memory since maximum size of the block is 9. For test case 1 each block of first cell is selected as base cell then the base cells are selected as 00, 03, 06, 30, 33, 36, 60, 63, 66 and the pattern are applied to the deleted neighborhood cells of each base cell. For test case 2 each block of second cell is selected as base cell then the base cells are selected 01, 04, 07, 31, 34, 37, 61, 64, and 67. Likewise for test case 9 the base cells are selected as 22, 25, 52 and 55.

6 III.

7 Memory Testing

8 Fig. 5: 8*8 memory divides into blocks

If base cell positions are not available in blocks then the base cells are chosen based on their availability [10]. Table 1 shows the base cells according to their respective test case.

9 c) Memory testing by using different test cases

10 d) Algorithm

Step 1: Write all base cells to 1.

Step 2: Applying pattern to neighborhood cells

11 e) Operation

During the 1st operation, cell 1 of each block will be selected as a base cell and the corresponding

12 b) Xilinx Reports

Xilinx ISE is a software tool is used for synthesis and analysis of HDL designs [11]. Allows the developer to synthesize the design, gives timing analysis, RTL diagrams, and configure the target device with a programming kit. The table 2 shows the summary of device utilization for Nexys 4 DDR Artx 7 FPGA. The utilization of device gives the information of number of LUTs, logic blocks and number of bonded IOBS used in FPGA, it can be obtained from synthesis report generated by Xlinx ISE.

V.

13 Conclusion and Future Scope

For memory arrays, the excessive test algorithmic time associated with NPSF fault model. This paper presents a BIST implementation using block code technique to select base cells and deleted neighborhood cells of neighborhood pattern sensitive faults (NPSFs) in random access memories (RAMs). Testing process is synthesized

and implemented on Nexys 4 DDR Artix 7 FPGA board. In order to improve the effectiveness of coupling faults, type-2 NPSFs can be modelled and tested. [1] [2]

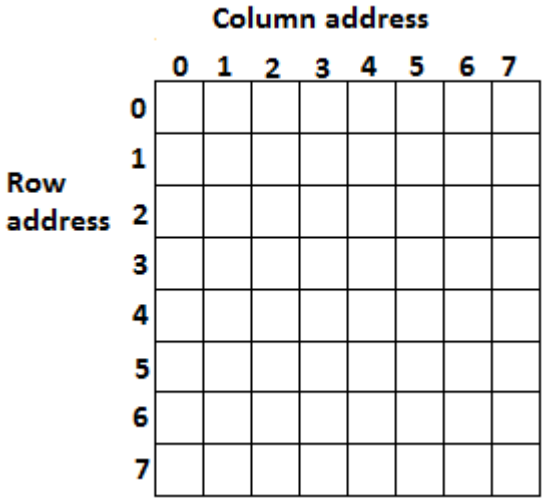

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Figure 1: Fig. 1 :

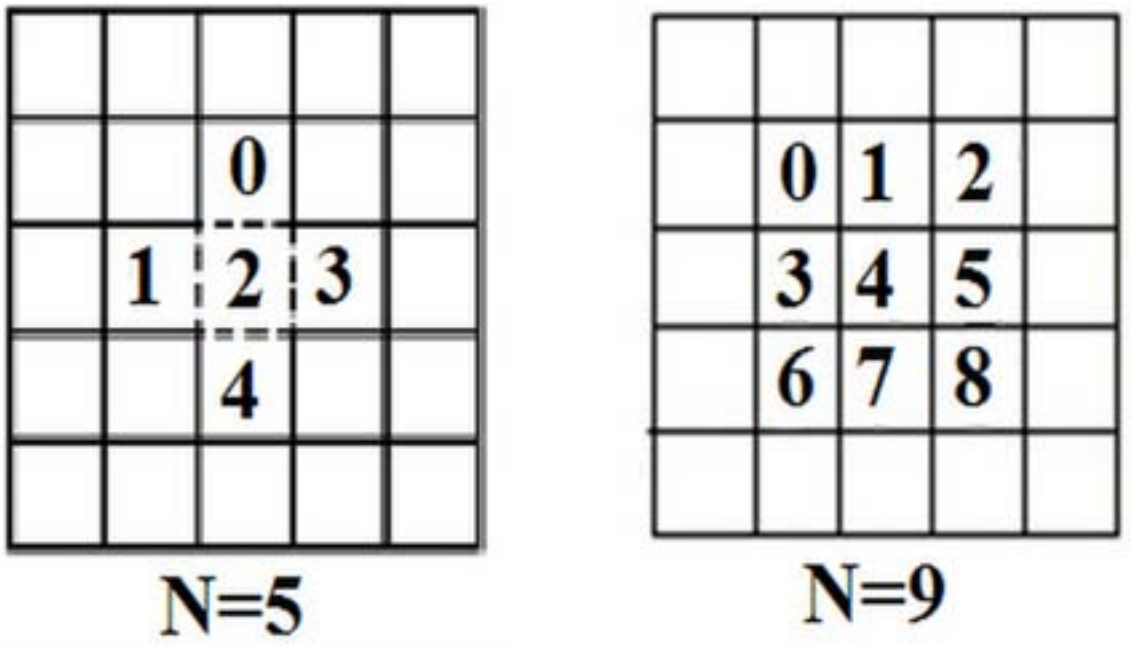

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Figure 2: Fig. 2 :

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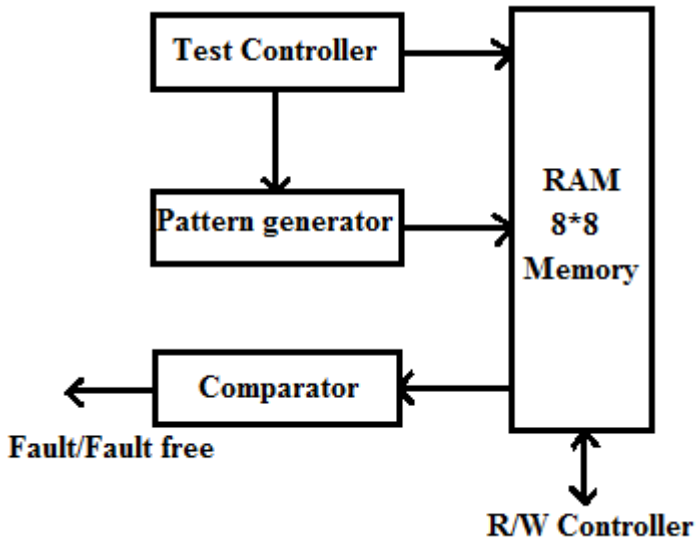

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Figure 3: Fig. 3 :Fig. 4 :

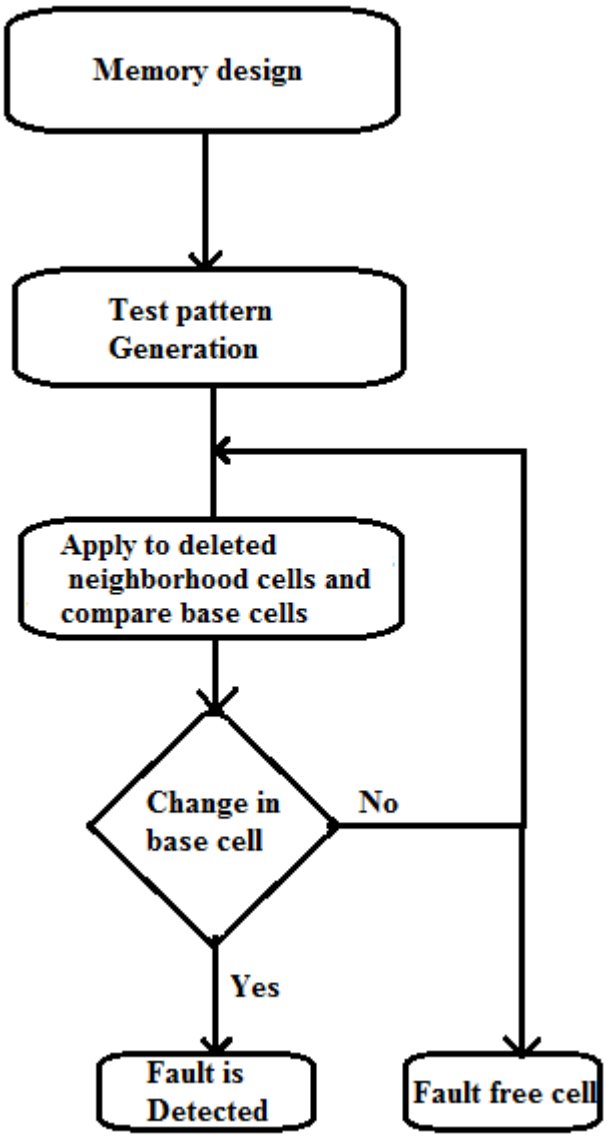

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Figure 4: Step 3 :

00	01	02	03	04	05	06	07
10	11	12	13	14	15	16	17
20	21	22	23	24	25	26	27
30	31	32	33	34	35	36	37
40	41	42	43	44	45	46	47
50	51	52	53	54	55	56	57
60	61	62	63	64	65	66	67
70	71	72	73	74	75	76	77

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Figure 5: Step 6 :Fig. 7 :Fig. 8 :Fig. 9 :

6

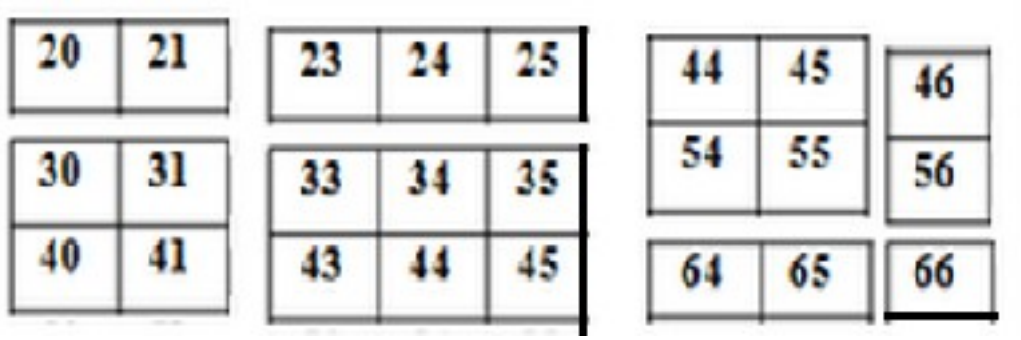

Figure 6: Fig. 6 :

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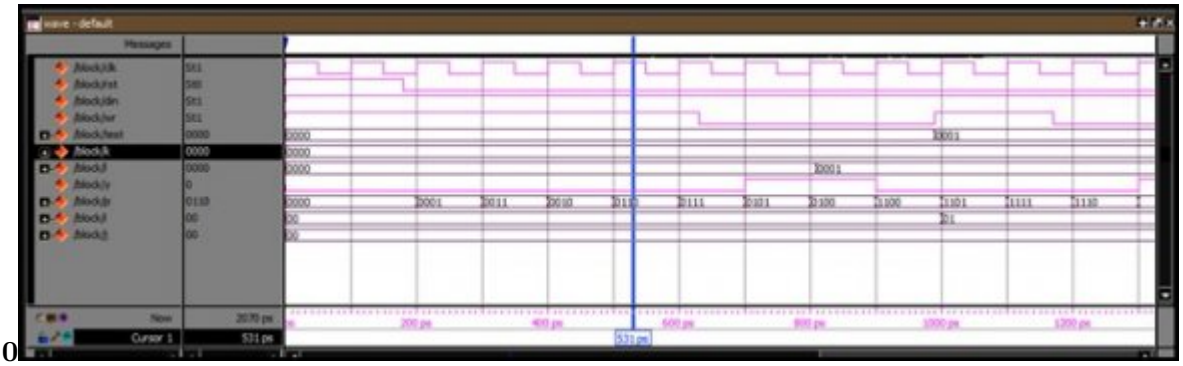

Figure 7: Fig. 10 :

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Figure 8: Fig. 11 :

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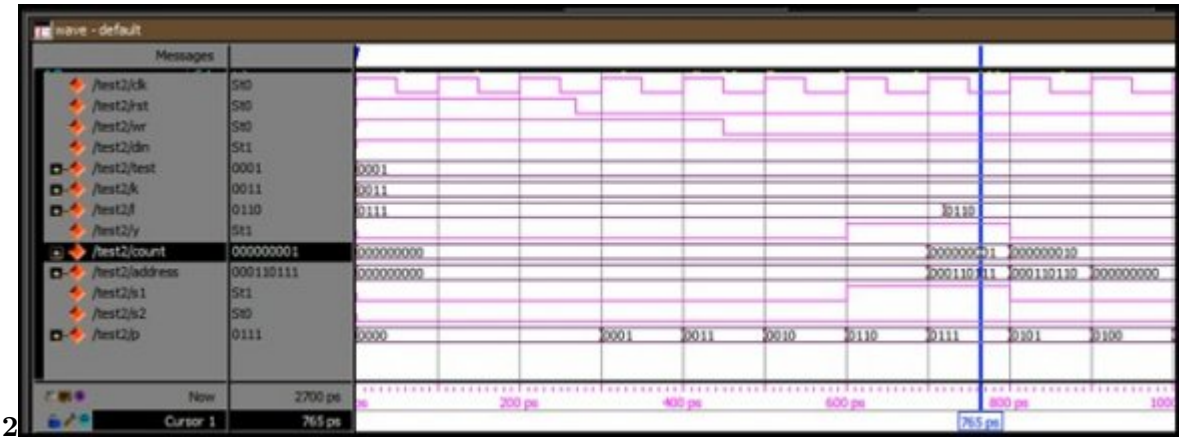

Figure 9: Fig. 12 :

1

Figure 10: Table 1 :

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Figure 11: Table 2 :

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