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Optimal High Performance Self Cascode CMOS Current Mirror

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OPTIMAL HIGH PERFORMANCE SELF CASCODE CMOS CURRENT MIRROR

Strictly as per the compliance and regulations of:

Optimal High Performance Self Cascode CMOS Current Mirror

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I. Introduction

To meet the needs of present era of low power portable electronic equipment, many low voltage design techniques have been developed. This led to the analog designers to look for innovative design techniques like Self cascode CMOS Current Mirror [1-5]. In this paper, we have investigated the merits and demerits of various current mirror configurations. For this we designed the basic current mirror first then improved our results by using various configurations like cascode current mirror, Wilson current mirror and finally the current mirror based on self cascode CMOS and analyzed its results through the SPICE simulations for 0.35 micron CMOS technology.

II. Basic MOSFET Current Mirror

The basic current mirror can also be implemented using MOSFET transistors (Fig: 1). Transistor M1 is operating in the saturation or active mode, and so is M2. In this setup, the output current IOUT is directly related to IREF, as discussed next. Simulation results for I_{out} vs V_{DS} curve for Basic Current Mirror is shown in fig 2. For a current mirror, neglecting channel length modulation:-

$$I_{out} = \tfrac{1}{2}\, \mu_n C_{ox} (W/L)_2 (V_{gs} - V_{th})^2 \qquad (1)$$

$$I_{ref} = \tfrac{1}{2}\, \mu_n C_{ox} (W/L)_1 (V_{gs} - V_{th})^2 \qquad (2)$$

When eq. 1 is divided by eq. 2, we have

$$I_{out} = I_{ref} (W/L)_2 / (W/L)_1$$

Limitations

1. As we can see from the basic current mirror circuit current gain is poor and the output current is having the channel length modulation effects. This is verified in eq. 3

$$I_{out} = I_{ref} \frac{(W/L)_2 (1+\lambda V_{ds2})}{(W/L)_1 (1+\lambda V_{ds1})} \qquad (3)$$

Here $V_{ds1} \neq V_{ds2}$.

2. Output resistance is finite and small value.

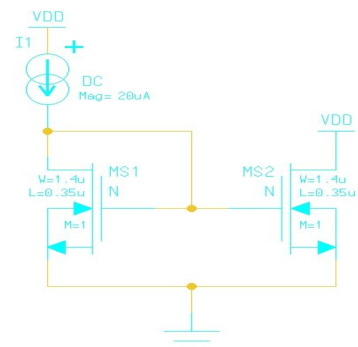

Fig 1: Basic current mirror

Simulation results:

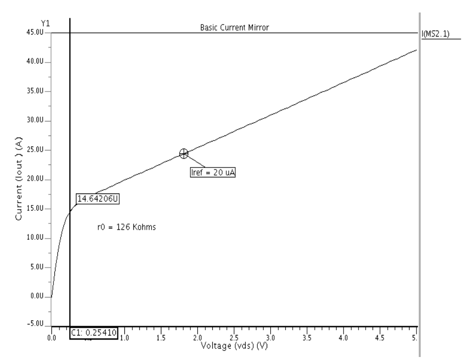

Fig 2 : I_{out} vs V_{ds} curve for Basic Current Mirror

III. Cascode Current Mirror

The idea of cascode structure is employed to increase the output resistance (Fig.3) and the implementation requires NMOS technology. It is used to remove the drawback of channel length modulation in basic current mirror. In the simulation results of basic current mirror the channel length modulation effect was not considered. In practice, this effect results in significant error in copying currents. The circuit features a wide output voltage swing and requires an input voltage of approximately one diode drop plus a saturation voltage. By maintaining the input transistors in saturation, the output current will track the input current, regardless of increases in ambient temperature [6, 7, 8].

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Simulation results for I_{out} vs V_{ds} curve for Cascode Current Mirror are shown in fig 4.

Advantages:

1. Cascode current mirror eliminates the channel length modulation effect by keeping Vds1 = Vds2 constant in the ratio:

$$Iout = Iref \frac{(W/L)\,(1+\lambda\, Vds_2)}{(W/L)\,(1+\lambda\, Vds_1)}$$

2. Improves output resistance.

Disadvantages

1. Less accurate.
2. Current becomes constant for quite large value of V_{ds} e.g. in this case minimum V_{ds} is 1.2 V.
3. Body effect is also present which disturbs the output current.

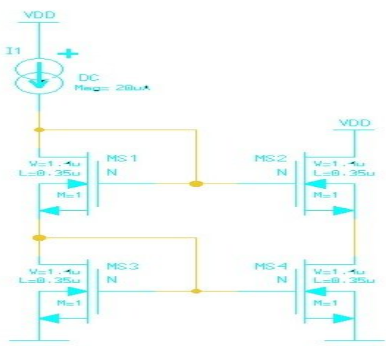

Fig 3 : cascode current mirror

Simulation results :

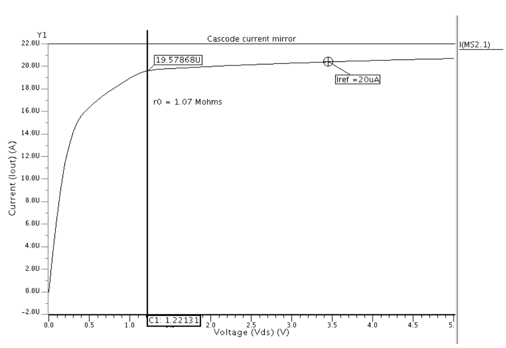

Fig 4 : I_{out} vs V_{ds} curve for Cascode Current Mirror

IV. Wilson Current Mirror

A Wilson current mirror or Wilson current source is a circuit configuration designed to provide a constant current (Fig:5). This circuit has the advantage of virtually eliminating the current mis-match of the conventional current mirror thereby ensuring that the output current I_{out} is almost equal to the reference or input current I_{Ref} thus eliminating the drawbacks of cascode structure. Simulation results for Iout vs V_{ds} curve for Wilson Current Mirror are shown in fig 6.

Advantages:

1. Curve is much flatter than basic and cascode current mirrors.
2. Output resistance becomes even much higher than cascode current mirror. This is caused by two positive feedback effects.

Disadvantages:

1. Current becomes constant for quite large value of Vds e.g. in this case minimum Vds is 1.22V.

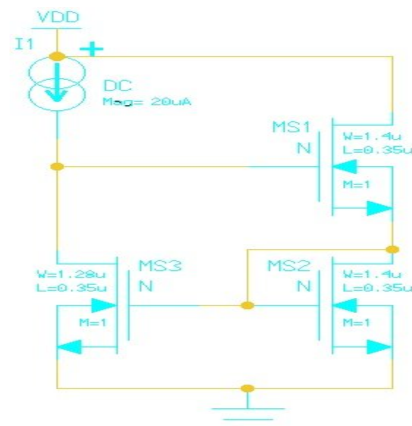

Fig 5 : Wilson current mirror

Simulation results:

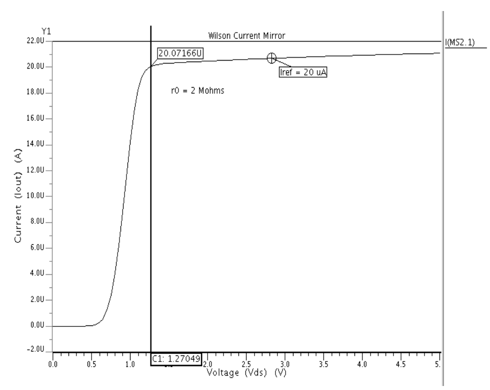

Fig 6 : I_{out} vs V_{ds} curve for Wilson Current Mirror.

V. Low Voltage Self Cascode Current Mirror

A self cascode current mirror is proposed that required a low bias voltage of order of ± 1.0V [9, 10]. The selection criterion for I_3 is to ensure lower V_{in}. I_2 is selected to ensure ON condition for M6 (Fig:7). The aspect ratios of different transistors are given in TABLE1. The small signal transfer analysis of this circuit at 20 μA gave the current gain, i.e. Iout/ Iin = 1, and output resistance as 10 MΩ. The power dissipation for this is high. Simulation results for I_{out} vs V_{ds} curve for Self Cascode Current Mirror are shown in fig 8. This approach of increasing the (*W/L*) aspect ratios works effectively at low bias voltage Vin of 1 V making it quite attractive for biasing analog circuits requiring high output resistance and gain. Hence they can be used as load resistances in CM circuits. They can extensively be used where power supply requirements are not the constraint.

Advantages:

1. High performance since output current is constant for low value of V_{ds}.
2. High output impedance.

Disadvantages:

1. Power dissipation is high.

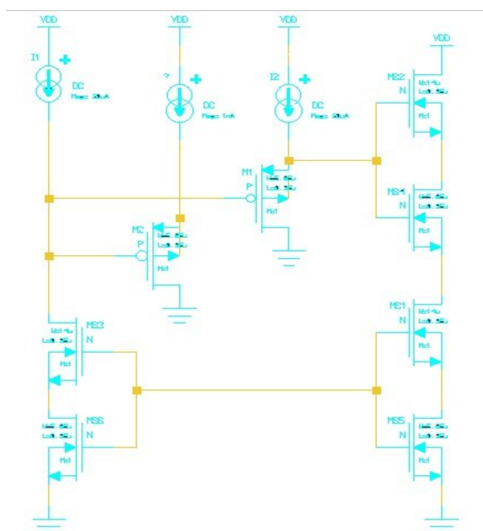

Fig 7 : Low voltage self cascode current mirror

I1, I2 = 20 n A

I 3 = 1 n A

V 2 = 1 V

Design specifications:

MOSFETs	Type	W/L
MS1,MS2,MS3	NMOS	70 to 14/0.35
MS4,MS5,MS6	NMOS	5.25/0.35
M1,M2	PMOS	5.25/0.35

Table 1 : aspect ratios of all MOSFETS

Simulation results:

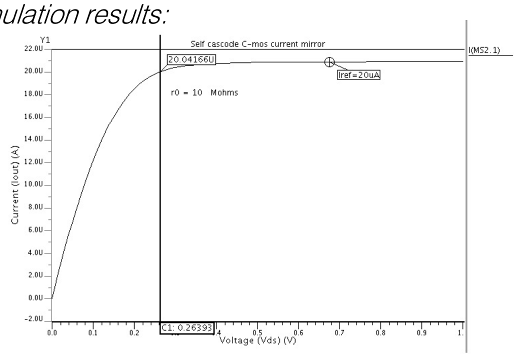

Fig 8 : I_{out} vs V_{ds} curve for Low voltage self cascode Current Mirror.

Comparision of different current mirrors:

A comparision of different current mirrors based on above simulation is given in TABLE 3. This TABLE compares the values of output impedence for each morror and the minimum output voltage required for running the circuit.

Current Mirrors	Stability	Output resistance	Min. output voltage(V)
Basic current mirror	Poor	126 K	0.254
Cascode current mirror	Good	1.07 M	1.22
Wilson current mirror	Better	2 M	1.27
Low voltage	Excellent	10 M	0.26

Table 3 : Comparison of different current mirrors

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