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Optimal High Performance Self Cascode CMOS Current Mirror

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Abstract

In this paper the current mirror presented, having low voltage and mixed mode structure has been proposed. The performance of self cascade MOSFET current mirror is optimized with high output impedance and can operate at 1 V or below. Simulation results conform to Analog Mentor tools having Design Architect for schematics and Eldonet for SPICE simulation, with input reference current of 20 ?A. This review paper presents a comparative performance study of self cascode current mirror with other current mirrors.

Index terms— current mirrors, cascode current mirror, low voltage analog circuit.

1 INTRODUCTION

o meet the needs of present era of low power portable electronic equipment, many low voltage design techniques have been developed. This led to the analog designers to look for innovative design techniques like Self cascode CMOS Current Mirror [1][2][3][4][5]. In this paper, we have investigated the merits and demerits of various current mirror configurations. For this we designed the basic current mirror first then improved our results by using various configurations like cascode current mirror, Wilson current mirror and finally the current mirror based on self cascode CMOS and analyzed its results through the SPICE simulations for 0.35 micron CMOS technology. 2 (1)

2 II.

3 BASIC MOSFET CURRENT MIRROR

I out = ½ ? n C ox (W/L) 2 (V gs -V th)I ref = ½ ? n C ox (W/L) 1 (V gs -V th) 2 (2)

When eq. 1 is divided by eq. 2, we haveI out = I ref (W/L) 2 / (W/L) 1

Limitations 1. As we can see from the basic current mirror circuit current gain is poor and the output current is having the channel length modulation effects. This is verified in eq. 3I out = I ref (W/L) 2 (1+?V ds2) (3) (W/L) 1 (1+ ?V ds1)

Here V ds1 ? V ds2 . 2. Output resistance is finite and small value.

4 CASCODE CURRENT MIRROR

The idea of cascode structure is employed to increase the output resistance (Fig. 3) and the implementation requires NMOS technology. It is used to T remove the drawback of channel length modulation in basic current mirror. In the simulation results of basic current mirror the channel length modulation effect was not considered. In practice, this effect results in significant error in copying currents. The circuit features a wide output voltage and requires an input voltage of approximately one diode drop plus a saturation voltage. By maintaining the input transistors in saturation, the output current will track the input current, regardless of increases in ambient temperature [6,7,8].

The basic current mirror can also be implemented using MOSFET transistors (Fig: 1). Transistor M1 is operating in the saturation or active mode, and so is M2. In this setup, the output current IOUT is directly related to IREF, as discussed next.

5 WILSON CURRENT MIRROR

A Wilson current mirror or Wilson current source is a circuit configuration designed to provide a constant current (Fig: 5). This circuit has the advantage of virtually eliminating the current mis-match of the conventional current mirror thereby ensuring that the output current I out is almost equal to the reference or input current I Ref thus eliminating the drawbacks of cascode structure. Simulation results for Iout vs V ds curve for Wilson Current Mirror are shown in fig 6 **??** Advantages:

1. Curve is much flatter than basic and cascode current mirrors. 2. Output resistance becomes even much higher than cascode current mirror. This is caused by two positive feedback effects.

Disadvantages:

1. Current becomes constant for quite large value of Vds e.g. in this case minimum Vds is 1.22V.

6 LOW VOLTAGE SELF CASCODE CURRENT MIRROR

A self cascode current mirror is proposed that required a low bias voltage of order of ± 1.0V [9,10]. The selection criterion for I 3 is to ensure lower V in . I 2 is selected to ensure ON condition for M6 (Fig: 7). The aspect ratios of different transistors are given in TABLE1. The small signal transfer analysis of this circuit at 20 ?A gave the current gain, i.e. Iout/ Iin = 1, and output resistance as 10 M?. The power dissipation for this is high. Simulation results for I out vs V ds curve for Self Cascode Current Mirror are shown in fig 8. This approach of increasing the (W/L) aspect ratios works Iref effectively at low bias voltage Vin of 1 V making it quite attractive for biasing analog circuits requiring high output resistance and gain. Hence they can be used as load resistances in CM circuits. They can extensively be used where power supply requirements are not the constraint.

Advantages:

1. High performance since output current is constant for low value of V ds . 2. High output impedance.

7 Disadvantages:

1. Power dissipation is high.

1

Figure 1: Fig 1 :

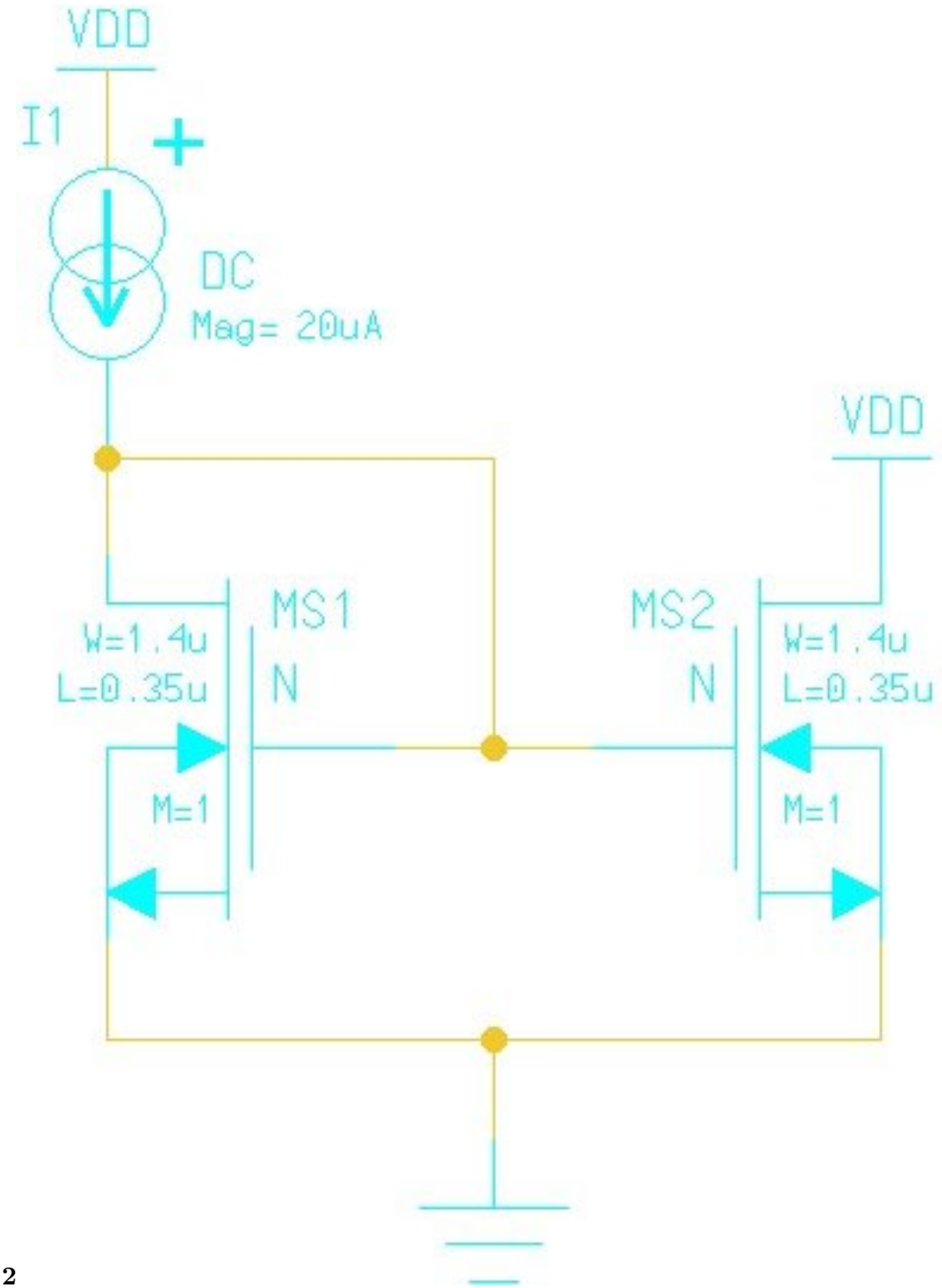

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Figure 2: Fig 2 :

7 DISADVANTAGES:

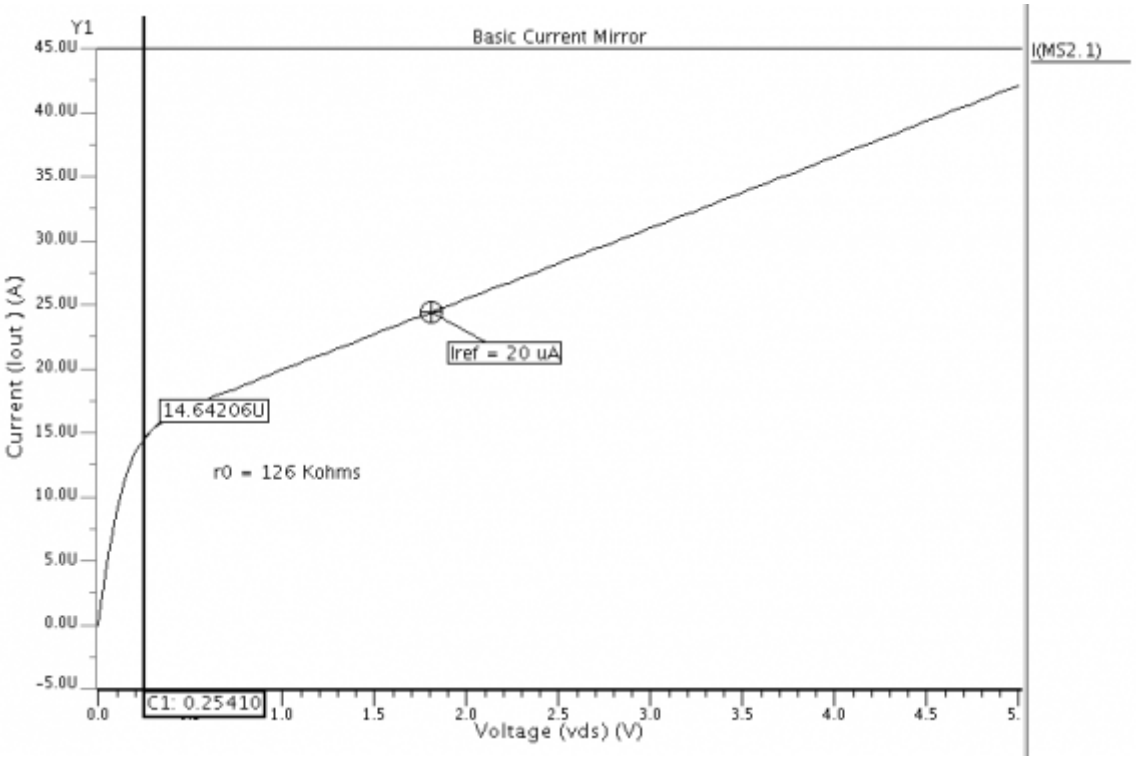

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Figure 3: 2 .

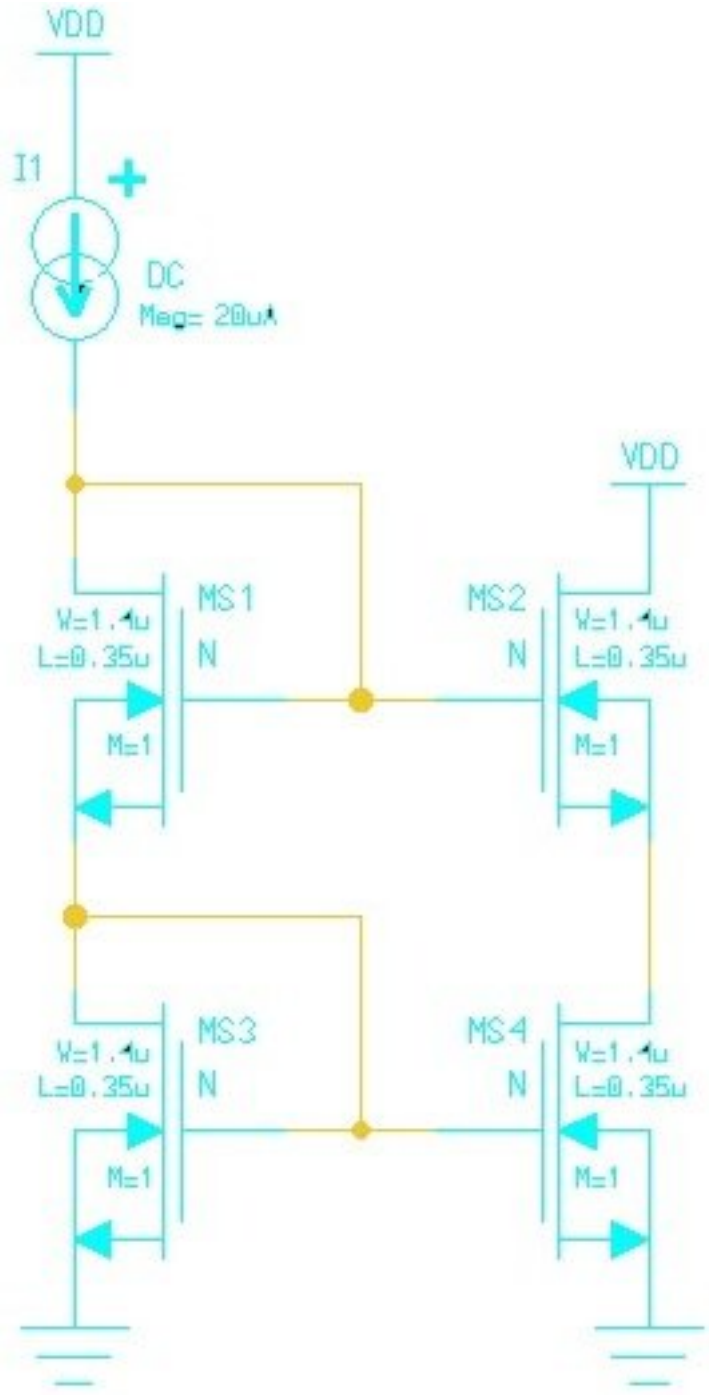

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Figure 4: Fig 3 :

7 DISADVANTAGES:

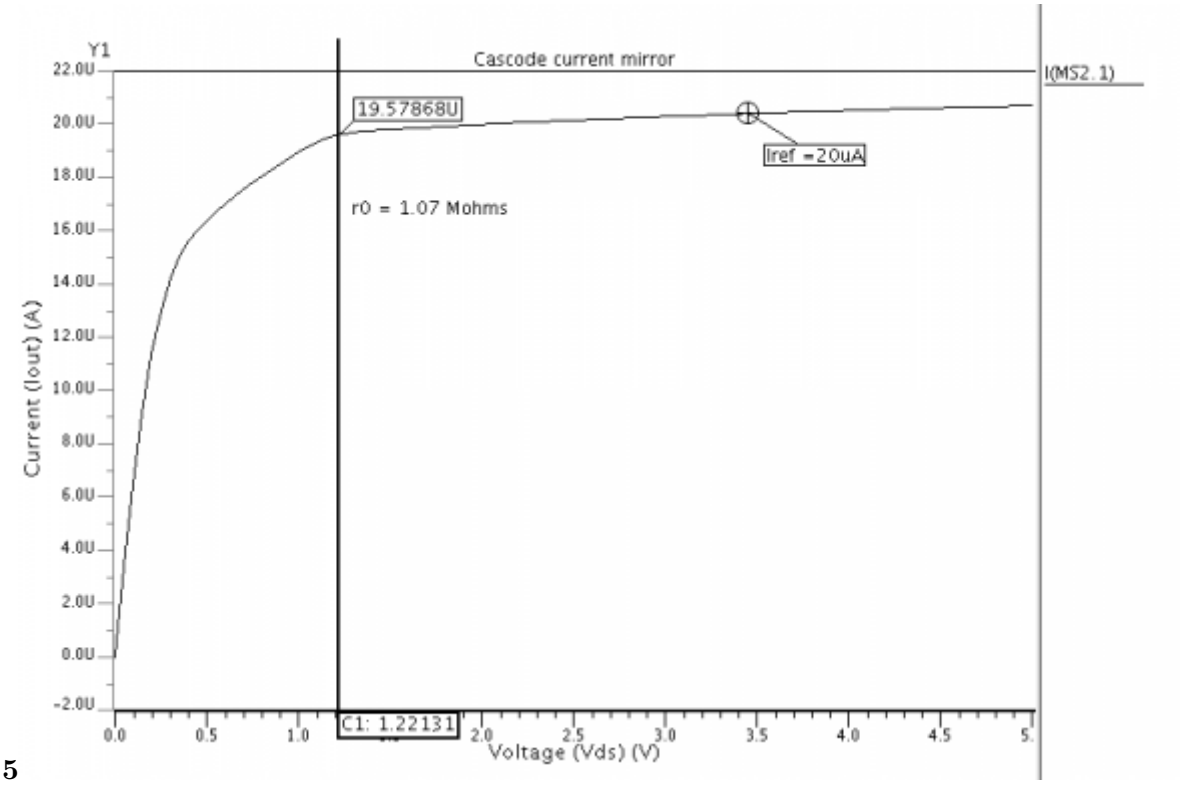

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Figure 5: Fig 5 :

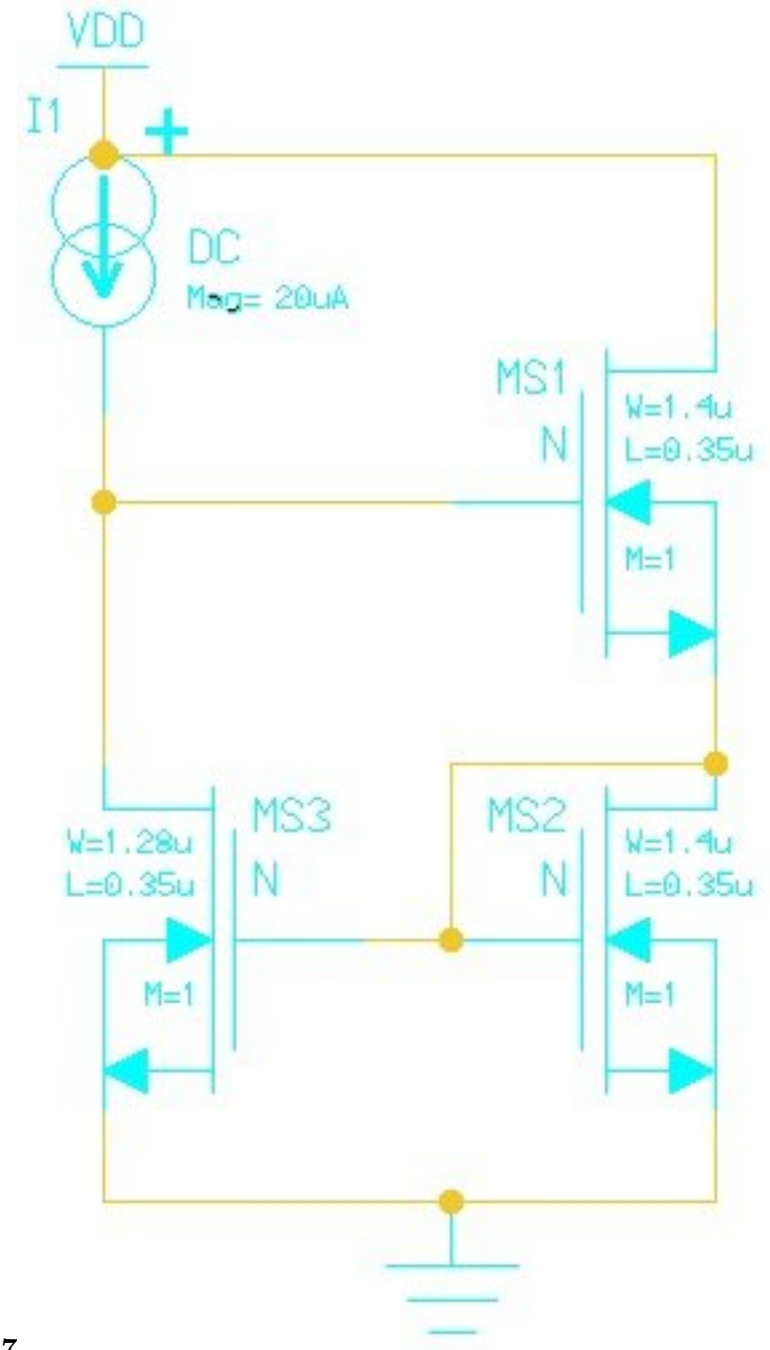

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Figure 6: Fig 7 :

Figure 7: Table

[Note: 1 : aspect ratios of all MOSFETS Design specifications:]

Figure 8:

3

2011
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63

[Note: vs V curve for Low voltage self cascodeCurrent Mirror.]

Figure 9: Table 3 :

[Rajput and Jamuar ()] 'A current mirror for low voltage, high performance Analog Circuits'. S S Rajput , S S Jamuar . *Proc. Analog integrated Circuits & Signal*, (Analog integrated Circuits & Signal) 2003. Kluwer Academic Publications. 36 p. .

[Sackinger and Guggenbuhl ()] 'A high swing, high impedance MOS cascode current mirror'. E Sackinger , W Guggenbuhl . *IEEE J. Solid State Circuits* 1990. 25 p. .

[Givstolisi et al. ()] 'A lowvoltage low power voltage reference based on subthreshold MOSFETs'. G Givstolisi , M Conscione , F Cutri . *IEEE J. Solidstate circuits* 2003. 38 p. .

[Razavi] *Design of Anlog CMOS Integrated circuits*, Behzad Razavi . (TMH edition 2002)

[Itakura and Czarnul ()] 'High output resistance CMOS current mirrors for low voltage applications'. T Itakura , Z Czarnul . *IEICE Trans. Fundamentals* 1997. (1) p. .

[Mulder et al. ()] 'High swing cascode MOS current mirror'. J Mulder , A C Woerd , W A Serdijn , A H M Roermund . *Electron. Lett* 1996. 32 p. .

[Shouli et al. ()] 'Low voltage Analog Circuit Design Techniques'. Yan Shouli , -Sinencio Sanchez , Edgar . *IEICE Transactions: Analog Integrated Circuits and Systems*, 2000. +A p. .

[Rajput and Jamuar ()] 'Low voltage analog circuit design techniques'. S S Rajput , S S Jamuar . *IEEE circuits systems Magazine* 2002. 2 p. .

[Rajput ()] *Low voltage current mode circuit structures and their applications*, S S Rajput . 2002. Delhi. Indian Institute of Technology (Ph.D. Thesis)

[Rincon and Gabriel (1995)] 'Low Voltage Design Techniques and Considerations for Integrated Operational Amplifier Circuit'. Alfonso Rincon , M Gabriel . *Georgia Institute of Technology* May 31. 1995. 30332.

[Xie et al. (1999)] 'Sound design of low power nested transconductance -capacitance compensation amplifiers'. M C Xie , E Schneider , S H K Sanchez-Sinencio , Embabi . *Electronic letters* June 1999. 35 p. .

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