Energy Efficient Network Generation for Application Specific NoC

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Abstract

Networks-on-Chip is emerging as a communication platform for future complex SoC designs, composed of a large number of homogenous or heterogeneous processing resources. Most SoC platforms are customized to the domainspecific requirements of their applications, which communicate in a specific, mostly irregular way. The specific but often diverse communication requirements among cores of the SoC call for the design of application-specific network of SoC for improved performance in terms of communication energy, latency, and throughput. In this work, we propose a methodology for the design of customized irregular network architecture of SoC. The proposed method exploits priori knowledge of the application?s communication characteristic to generate an energy optimized network and corresponding routing tables.

Index terms— SoC, on-chip networks, application specific NoC, design methodologies, Mesh topology, interconnection network.

1 INTRODUCTION

he shrinking feature sizes in silicon technologies is making possible the integration of complex systems-on Chip (SoC), offering a remarkable amount of computational power. In order to address the design complexity and assist reuse, these systems are usually built from predesigned and preverified building blocks like general-purpose processor, a DSP, a memory subsystem, etc. Functionality of these systems is generally captured by a set of communicating tasks at a high level of abstraction. These tasks are mapped to computational resources which are interconnected by an underlying communication infrastructure.

or regular based on their underlying communication infrastructure / topology. This communication infrastructure or topology impacts both performance and implementation costs of the system in terms of silicon area and energy consumption to a substantial extent.

A large number of NoC architectures have been proposed based on regular building patterns ; Kumar, Jantsch, Soininen, Forsell, Millberg, Oberg, Tiensyrja & Hemani, 2002; Natvig, 1997) like meshes, tori, k-ary n-cubes or fat trees for the implementation of on-chip networks to overcome conventional bus-based designs. However regular topologies may not be appropriate where communication requirement are not uniformly distributed across cores and links. Moreover most application specific SoCs are designed with static (or semi-static) mapping of tasks to processors or hardware cores and consequently the communication requirements of the SoC can be well characterized at design time. Therefore, the NoCs with irregular topology customized to the application's requirements is expected to be the preferred choice for application specific SoC platforms.

The routing function in NoC based systems is tightly coupled to the underlying topology defining the set of allowed paths on which packets may be sent from a sender to the destination core. The proper selection of the adequate topology and routing function form a key decision in the design of the overall NoC architecture. Conventionally, the proof of deadlock-freedom has mostly been carried out on the assumption of the regular topology (Dally & Seitz, 1987;Glass & Ni, 1992;Duato, Yalamanchili & Ni, 2003) and is far more complicated for NoC with underlying irregular topology. However in the NoC research domain some routing functions based on turn prohibition (Glass & Ni, 1992) methodology are proposed for irregular topology based NoCs such as prefix

routing (Wu & Sheng, 1999), up*/down* (Schroeder et al. 1991), Left-Right (Jouraku, Funahashi, Amano & Koibuchi, 2001), L-turn (Jouraku, Funahashi, Amano & Koibuchi, 2001) and down/up (Sun, Yang, Chung & Hang, 2004).

In this paper, two genetic algorithm based heuristics are proposed for the design of energy efficient customized irregular topology Networks-on-Chip based on the applied routing function for application having IP cores with varying communication bandwidth requirements. The presented methodologies exploit the predefined communication requirements of the application to generate energy efficient customized NoC along with the routing tables for supporting deadlock free communication. It is worth mentioning here that the topology and routing table generation are tightly coupled aspects of the NoC design and therefore optimization of only one aspect or one after another may lead to suboptimal solutions. The paper is organized as follows. A brief account of related work is presented in Section II. Communication model and architecture for Irregular NoC are defined in Section III. The proposed genetic algorithm based energy efficient NoC design methodologies are presented in Section IV. The Genetic Algorithm used in the proposed methodologies is described in Section V. Experimental results are presented in Section VI followed by a brief conclusion in Section VII.

2 II.

3 RELATED WORK

Methods to collect and analyze traffic information that can be fed as input to the bus and NoC design processes have been presented in (Lahiri et al. 2004) and (Murali & De Micheli, 2005). Mappings of cores onto standard NoC topologies have been explored in (Murali & DeMicheli, 2004;Hansson et al. 2005;Hu & Marculescu, 2003;Murali et al. 2005). In (Murali & DeMicheli, 2004;Murali et al. 2005) a floorplanner is used during the mapping process to get area and wire-length estimates. These works only select from a library of standard topologies, and cannot generate a fully customized topology. In (Hansson et al. 2005), a unified approach to mapping, routing and resource reservation has been presented.

However, the work does not explore the topology design process. Important research in macro networks has considered the topology generation problem (Ravi et al. 2001). As the traffic patterns on these networks are difficult to predict most approaches are tree-based (like spanning or Steiner trees) and only ensure connectivity with node degree constraints. These techniques cannot be directly extended to address the NoC synthesis problem.

Application-specific custom topology design has been explored in (Pinto et al. 2003;Ho & Pinkston, 2003;Ahonen et al. 2004;Srinivasan et al. 2005). The works from (Pinto et al. 2003;Ho & Pinkston, 2003), do not consider the floorplanning information during the topology design process. In (Ahonen et al. 2004), a floorplanner is used during topology design to reduce power consumption on wires. It does not consider the area and power consumption of switches in the design. Also, the number and size of network partitions are manually fed. In (Srinivasan et al. 2005), a slicing tree based floorplanner is used during the topology design process. This work assumes that the switches are located at the corners of the cores and does not consider the network components (switches, network interfaces) during the floorplanning process. Actual sizes of the cores in (Srinivasan et al. 2005; Srinivasan, & Chatha 2005) are considered only after generating their relative positions. The resulting floorplan can be extremely area inefficient when compared to the standard floorplanning process. In (Choudhary, N et al. 2010), a methodology to generate Bandwidth Aware NoC topology according to the application requirement is proposed. This methodology does floorplanning as the first step with high priority and later accomplishes topology generation with better traffic load distribution across the channels of the NoC leading to reduced congestion as well as hot spots in the topology. A range of issues in the design methods and tools for efficient synthesis of application specific Network-on-Chip interconnect for 3D SoC were addressed in .

In addition to the above, one of the major challenges for successful adoption of the Network-on-Chip paradigm is in reducing the energy consumed during the interaction between the IP cores. In (Hu & Marculescu, 2003;, Hu and Marculescu have presented an energy-aware mapping algorithm to minimize the total communication energy cost for a 2-D mesh NoC architecture under real-time performance constraints. Similarly in (Choudhary, N., Gaur, M. S., Laxmi, V., Singh, V. (2010)) a deterministic methodology of order O(n2) to generate energy efficient NoC topology is proposed. This methodology also does floorplanning as the first step with highest priority as in (Choudhary, N et al. 2010). However due to its deterministic nature the methodology is not capable to generate energy optimized NoC topology for all the given applications. The work in (Choudhary, N., Gaur, M. S., Laxmi, V., Singh, V. (**??**010 Definition 2 : NoC topology graph is a directed graph N (U, F) with each vertex ?i ?U representing a node/tile in the topology and a directed edge fi,j ?F represents direct communication channel between vertices ?i and ?j. Weight of the edge fi,j denoted by bi,j represents the available link/channel bandwidth across the edge fi,j.

The energy model (Hu & Marculescu, 2003) for the regular Network-on-Chip can be defined as Follows : (1) Where E bit (t i , t j) is the average dynamic energy consumption for sending one bit of data from tile ti to tile t j , n hops is the number of routers the bit traverses from tile t i to tile t j , Er bit is the energy consumed by router for transporting one bit of data and El bit is the energy consumed by link/channel for transporting one bit of data. In case of Irregular NoC with unequal length (2) Where the 2nd term of the summation in equation (**??**) represent the bit energy consumed by each channel in the route, the bit follows from communication source core to the intended destination cores.

For optimized chip layout, floorplanning according to desired metric like area can be done as a first step with the help of available floorplannning tools such as B*-Trees (Chang, Chang, Wu & Wu, 2000; Lin & Chang, 2005).

The presented work uses the escape path based routing function as proposed by (Silla & Duato, 2000). To provide deadlock free communication in the NoC, the up*/down* routing (Schroeder et al. 1991;Silla et al. 1997) and Left-Right routing (Jouraku, Funahashi, Amano & Koibuchi, 2001) were used. These routing functions assign direction to the channels of the NoC with the help of a spanning tree of the give NoC topology.

In (Silla & Duato, 2000), a generic methodology for designing adaptive routing function for Irregular NoC was proposed. The proposed methodology allow messages to follow minimal paths, in most cases, reducing message latency and increasing network throughput (Duato, Yalamanchili & Ni 2003). Moreover the methodology enforces the deadlock free route to be followed only when the minimal path is occupied by other traffic/packet. This methodology assumes that all the physical channels in the NoC can be split into two virtual channels i.e. original virtual channel and the new virtual channel. Moreover the presence of a given deadlock free routing functions based on turn prohibition (Glass & Ni, 1992) for the given irregular NoC is also assumed. The methodology further proposes to extend the given routing function in such a way that newly injected messages can use new channels without any restriction as long as the original channels are used exactly in the same way as in the original routing function. In this paper original channels are made to use deadlock free paths based on up*/down* (Left-Right) deadlock free routing functions and new channels are allowed to follow the shortest available path to the destination. The modified routing function allows a packet arriving on a new channel following shortest path to be routed to any channel without any restrictions but preferably with higher priority to new channels as new channel assure shorter paths and higher adaptively (flexibility). If no new channels are available due to congestion, one of the original channels following up*/down* (Left-Right) must be provided. However, once a packet acquires an original channel following up*/down* (Left-Right) path, it is not allowed to do transition to a new channel anymore to avoid deadlock situation. Assuming over the cell routing (Srinivasan & Chatha, 2006), the link length among the nodes in the chip layout can be taken according to Manhattan distance. In both the proposed methodologies, the link/channel length is not allowed to exceed the maximum permitted channel length (e max) due to constraint of physical signaling delay. This also prevents the algorithm from inserting wires that span long distances across the chip. Also, the nodes of the generated topology are not allowed to exceed a given maximum permitted node-degree (nd max). This constraint prevents the algorithm from instantiating slow routers with a large number of I/O-channels that would otherwise decrease the achievable clock frequency due to internal routing and scheduling delay of the router.

4 IV. DESIGN METHODOLOGIES FOR ENERGY EFFICIENT NOC GENERATION

5 a) Minimum Spanning Tree First (MSTF) Methodology

In this proposed methodology to generate the energy efficient customized topology, first a minimum spanning tree (MST) using Prim's algorithm (Cormen, Leiserson & Rivest, 1990) is generated on the nodes of the Core Graph according to information regarding the Manhattan distance from the floorplan with the constraints on nd max and e max . The node/core with maximum bandwidth requirement is assumed as the root of the tree. The minimum spanning tree in the topology helps us in classifying all the channels/links of the topology as "up" ("Left") or "down" ("Right"). The following phases of MSTF methodology helps in extending the network/topology for energy efficient deadlock free communication.

Aware Topology Extension Phase : While keeping the constraints on nd max and e max , the topology is further extended by laying the shortest energy path for each traffic characteristics (edges corresponding to pair of nodes in the Core Graph). Due to constraints on nd max and e max , the order in which such shortest energy paths are generated basically decides the total communication energy requirement of the generated topology. The optimized order of traffic characteristics of the application is found using a genetic algorithm (refer next section). The routing tables of nodes/routers in the discovered shortest energy path are updated with the routing table entry type tag as shortest path.

Deadlock Avoidance Phase : Lastly the proposed methodology uses the modified Dijkstra's algorithm (Cormen, Leiserson & Rivest, 1990) according to up*/down* (Left Right) rule for finding deadlock free escape routing paths from each node in the shortest energy path to the corresponding destination in the generated NoC and tags them as up*/down* (Left-Right).

While taking routing decision the output channels tagged as shortest path are selected with higher priority and up*/down* (Left Right) tagged channels are selected only when no output channel corresponding to shortest path is free. b) Shortest Path First (SPF) Methodology SPF is similar to MSTF methodology with the exception that in SPF the topology generation is initiated by first finding the shortest energy path and later the topology is extended by constructing the MST. As in Energy Aware Topology Extension Phase of MSTF, a genetic algorithm is used to find the optimized energyefficient traffic characteristics order of the application. Since in MSTF, MST is constructed first, it is possible that a large number of links for a number of nodes/cores in the topology are the links pertaining to MST. As maximum links emanating from a node is limited to ndmax, this phenomenon can lead to increased value of hop count in the shortest energy paths generated later leading to increased communication

energy. However the SPF overcomes this drawback by creating the links pertaining to shortest energy path before the links September pertaining to MST. As shortest energy paths in the topology are generated first in SPF and so there can be a possibility that not enough number of free ports is available to construct the MST in the topology later. In such case a minimum number of ports per node/core need to be reserved before finding the shortest energy paths. However experiments showed that if communication requirement are uniformly distributed over the Core Graph then such problems are rare if any. Algorithm 1 briefly presents the proposed methodologies.

6 VII. GENETIC ALGORITHM

A genetic algorithm (Eiben & Smith, 2003) based heuristic is used to find the best order of the traffic characteristics to generate the shortest energy paths in topology such that the communication energy requirement of the application is optimized. Genetic algorithm is a search technique used in determining exact or approximate solutions to optimization and search problems. Genetic algorithms are a particular class of evolutionary algorithms which uses techniques inspired by evolutionary biology such as inheritance, mutation, selection, and crossover. The proposed genetic algorithm explores the search space extensively to generate an irregular topology with optimized communication energy requirement for the given application. The proposed genetic algorithm formulation is as follows.

7 a) Solution Space

In formulation of the proposed methodology, each chromosome is represented as an array of genes. Maximum size of the gene array is equal to the number of edges in the Core Graph. Each gene of the chromosome represents a traffic characteristic (an edge corresponding to a pair of nodes in the Core Graph) b) Initial Population A large population (i.e. 500 chromosomes) of chromosome is initially generated. The chromosomes of the initial population are generated by assigning traffic characteristics of the application to the chromosome's gene array in some random order. The initial population is later sorted according to the increasing order of total communication energy requirement of the generated topology (chromosome). It is worth highlighting here that the communication energy consumption by a chromosome varies depending on the traffic characteristics order (order of elements in gene array) of the chromosome.

8 c) Crossover

In each generation, crossover is performed on 50% of the population with the bias towards the Best Class of the chromosome population. For achieving crossover of two chromosomes, a random crossover point is selected. Two new chromosomes are created by the crossover operation. The new chromosomes are created by copying the traffic characteristics (genes) from their respective parents till crossover point or from crossover point to the end of the chromosome and then the remaining traffic characteristics (genes) are copied according to the order of traffic characteristics (genes) in the other chromosome such that there are no duplicate traffic characteristics in the created chromosomes.

9 d) Mutation

In each generation, mutation is performed on 40% of the population to avoid the solution from getting stuck up in the local minima. Two types of mutations with probability of 50% each are performed in each generation. In first type of mutation a gene in the gene array of the chromosome with highest energy requirement is swapped with a randomly selected gene of the chromosome. In second type two randomly selected genes in the gene array of the chromosome are swapped.

10 e) Measure of Fitness

The cost function used to measure the fitness of the chromosomes in the population can be formulated as under.

Where X is maximum chromosome energy requirement among all the chromosomes in the population, Ec i is the energy requirement for chromosome c i . Fitness of chromosome is regarded as high if its cost approaches 0. It may be noted that, the best 10% chromosomes (referred as Best Class) in any generation are directly transferred to the next generation so as not to degrade the solution between the generations.

Algorithm 2 briefly presents the proposed genetic algorithm formulation. After genetic algorithm methodology is made to run for a required number of generations, the NoC topology and routing tables corresponding to the best output chromosome are accepted as the customized energy optimized application specific NoC.

11 VIII. EXPERIMENTAL RESULTS

The generated energy aware application specific topology was evaluated with respect to the communication energy consumption with applied traffic load on the NoC simulation framework. In order to obtain a broad range of different irregular traffic scenarios, multiple Core Graphs using TGFF (Dick, Rhodes & Wolf, 1998) were randomly generated with diverse bandwidth requirement of the IP Cores. For performance comparison, a NoC simulator IrNIRGAM, the extended version of NIRGAM (Jain, Al-Hashimi, Gaur, Laxmi & Narayanan, 2007; Jain 2007) supporting irregular topology with the provision of supporting escape path routing for avoiding

deadlock condition, was deployed. IrNIRGAM is a discrete event, cycle accurate simulator. IrNIRGAM supports irregular topology framework with source and table based routing in a wormhole switching based architecture wherein an IP Core is directly connected to a dedicated router. In IrNIRGAM, input buffered routers can have multiple virtual channels (VCs) and uses wormhole switching for flow control. The packets are split into an arbitrary number of flits (flow control units) and forwarded through the network in a pipelined fashion. A Round-Robin scheme for switch arbitration is used in the router nodes to provide fair bandwidth allocation while effectively preventing scheduling anomalies like starvation.

For performance comparison on experimental set, the IrNIRGAM was run for 10000 clock cycles with applied packet injection interval to evaluate the network performance with varying traffic load. The energy consumption by the flits reaching their corresponding destination and flit latency were used as performance metric. The energy consumption by routerX Ec Cost i / =

in transmitting a bit is evaluated using the power simulator orion (Kahng, Li, Peh & Samadi, 2009) for 0.18?m technology. Similarly the dynamic bit energy consumption for inter-node links (Elbit) can be calculated using the following equation.

Where ? is the average probability of a 1 to 0 or 0 to 1 transition between two successive samples in the stream for a specific bit. The value of ? can be taken as 0.5 assuming data stream to be purely random. Cphy is the physical capacitance of inter-node wire under consideration for the given technology and VDD is the supply voltage. Figure 7 shows that SPF consistently performs better in comparison to BA-TGM as far as average dynamic communication energy consumption by flits reaching their destination is concerned. The SPF showed on average a reduction of 38.6% for the communication energy per flit in comparison to BA-TGM.

12 CONCLUSION

In this paper, the energy efficient customized Irregular topology generation problem for NoC was addressed. Two genetic algorithm based novel methodologies are proposed for generating the NoC topology with optimized communication energy requirements according to the traffic characteristics of the given application. Although in this paper up*/down* and Left-Right routing were used as escape path for deadlock prevention, we argue that the proposed methodologies can be adapted with any of the topology agnostic routing algorithms where generic routing rules based on turn prohibition can be enforced. It is believed that the combined treatment of the routing and topology generation as done in the presented methods offers a huge potential of optimization for future applicationspecific NoC architectures. Some interesting extensions of the proposed design can be to combine the topology generation with the task partitioning/scheduling into the presented framework to make the design more adaptable to the dynamic communication requirement of the application in such a way that the computation and communication energy consumption can be optimized at the same time. [1] [2] [3] [4]

Figure 1:

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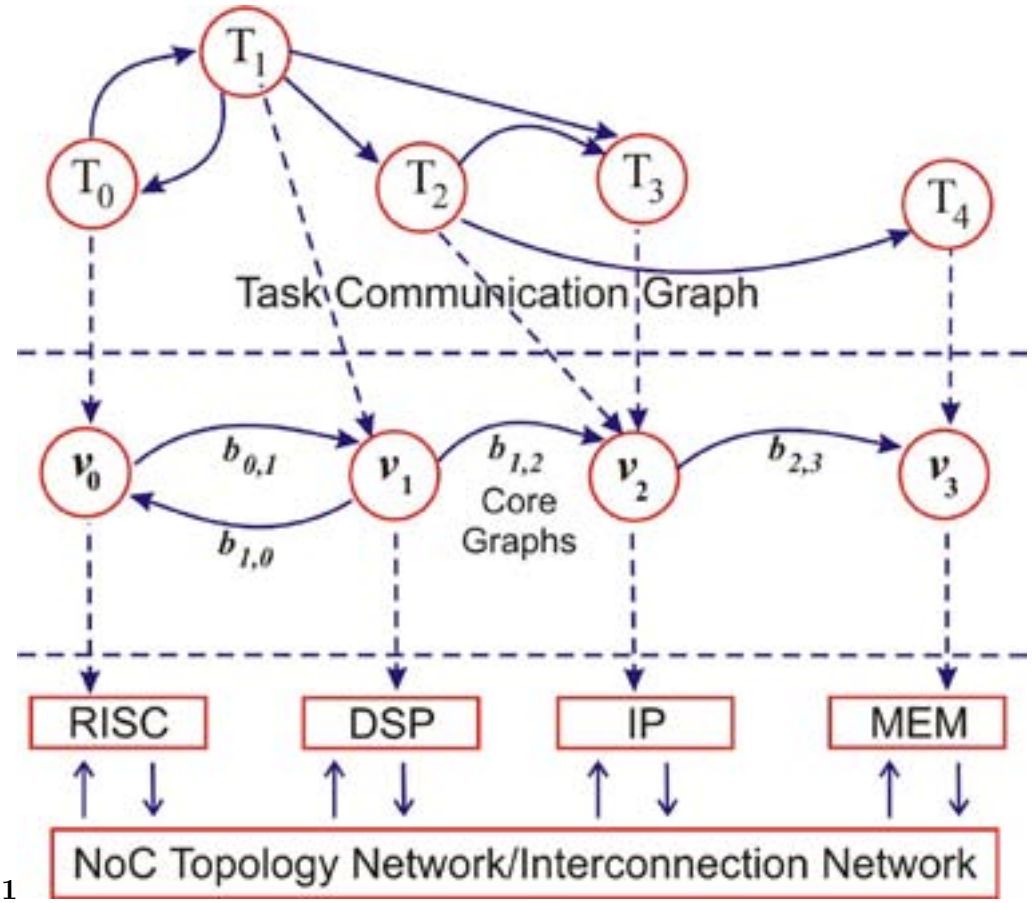
[3] SeptemberEnergy Efficient Network Generation for Application Specific Noc

[4] © 2011 Global Journals Inc. (US) Global Journal of Computer Science and Technology Volume XI Issue XVI Version I 52



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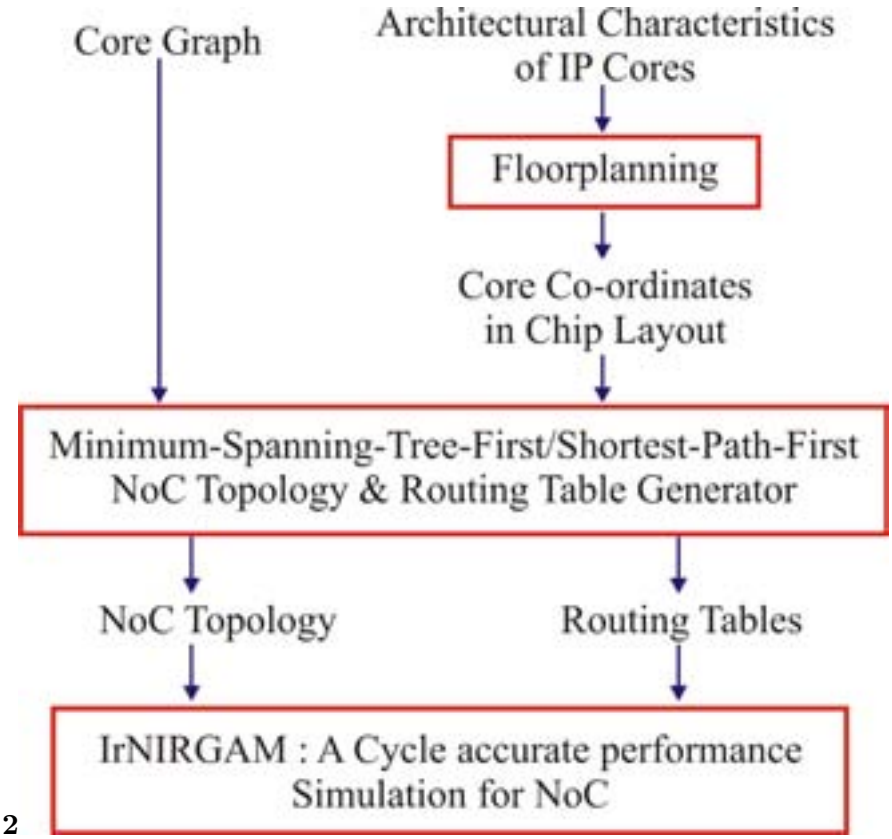

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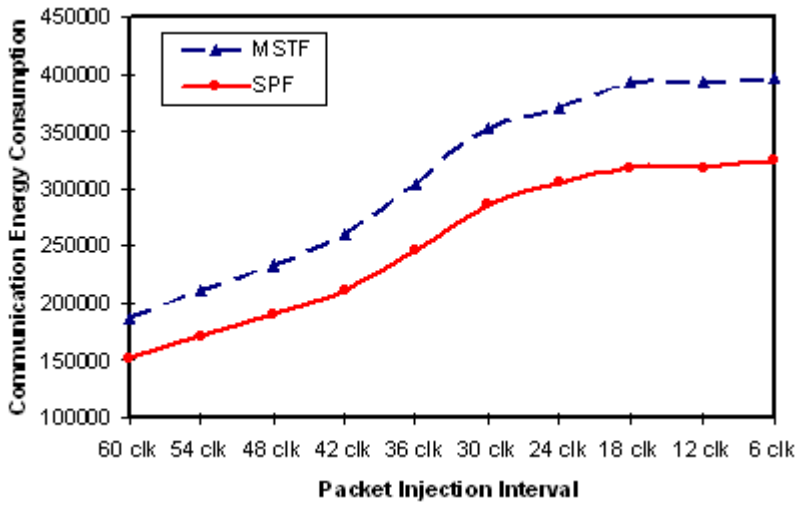
Figure 3: Fig. 2 :



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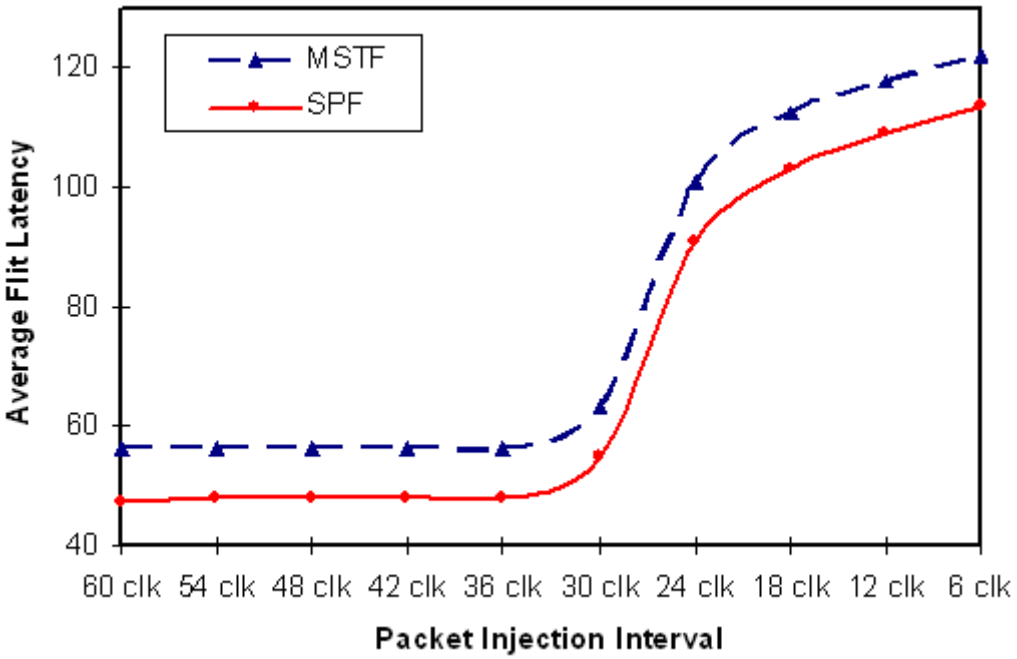

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Figure 5: Algorithm 1 :

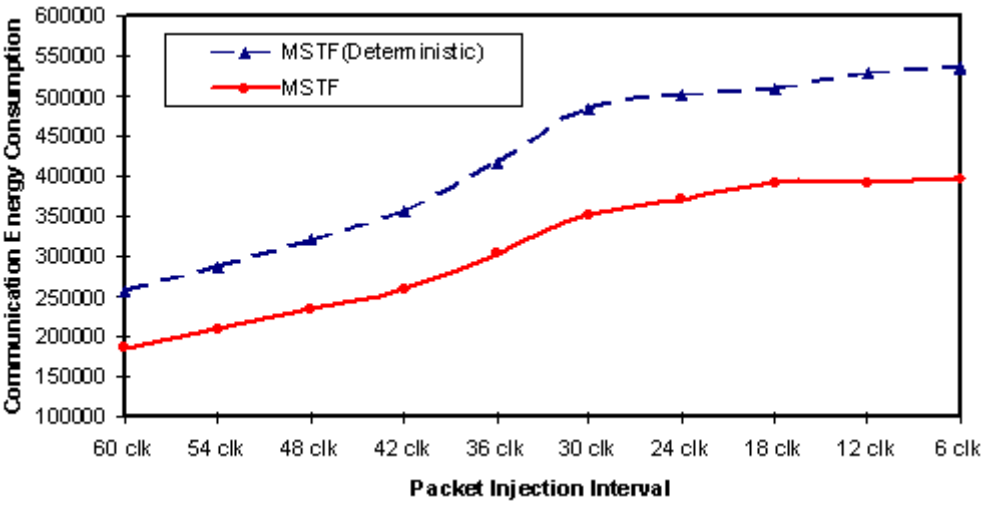

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Figure 6: Algorithm 2 :

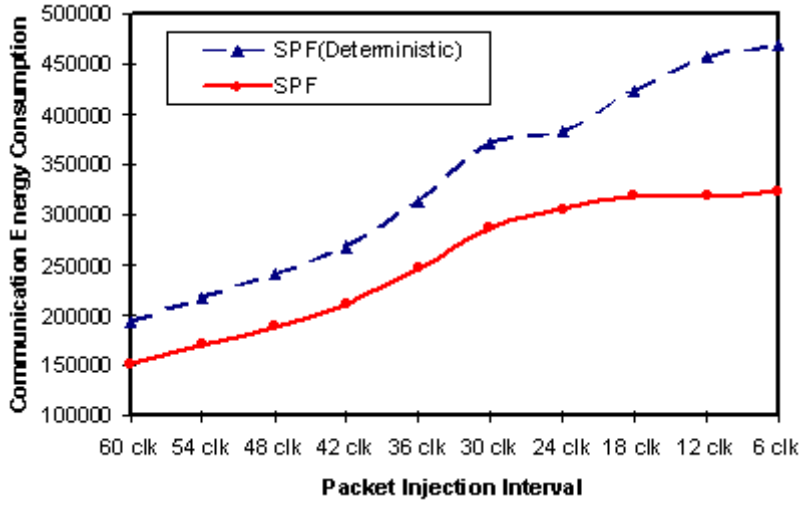

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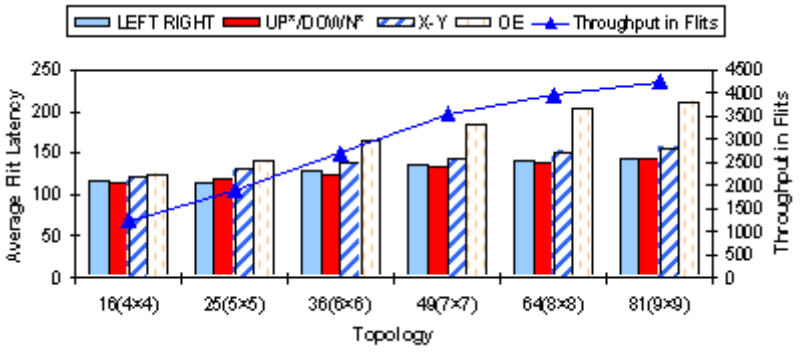
Figure 7: Fig. 3 :



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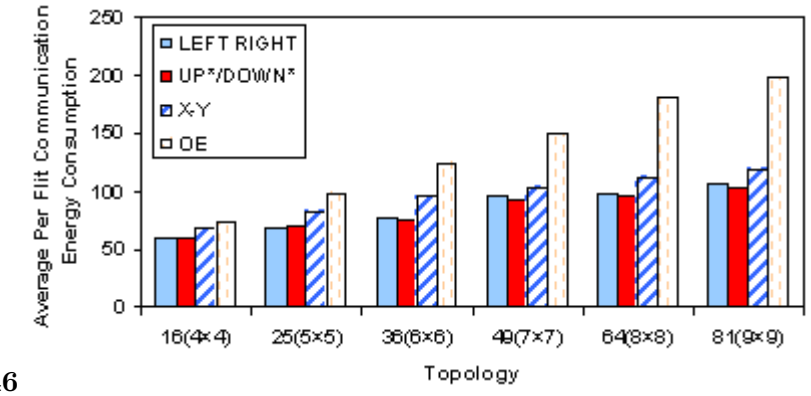

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Figure 9: Figure 4 showsFig. 6 :

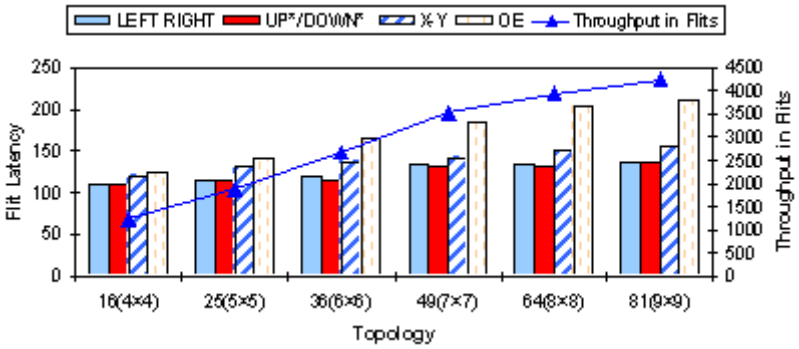

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Figure 10: Figure 6

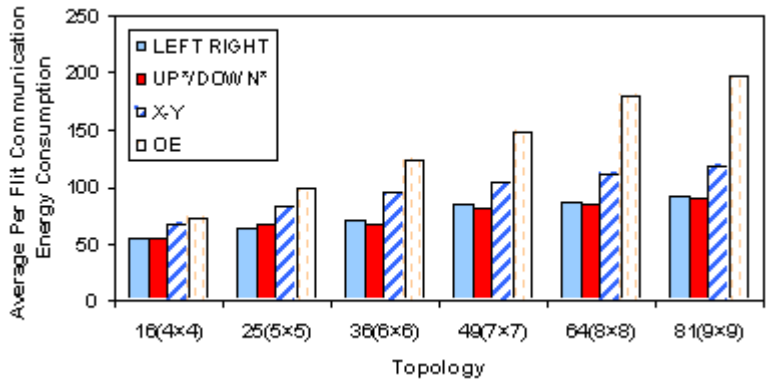

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Figure 11: Fig. 7 :

entry

type tag is set as up*/down* (Lef -Right) for these nodes} Endprocedure o endfor ? endfor Procedure Shortest-Paths-First ( ) ??? ? .NoC EA ; // initialize the energy aware NoC (i.e. NoC EA) ? NoC is set as up*/down* (Lef -Right) for these nodes} o endfor ? endfor endprocedure

[Note: EA .T = ?; NoC EA .R = ?; NoC EA .S = ?; ? Î?” = ? ; ? (NoCEA, TC_Array) = GeniticAlgo(NoC EA ,Î?”) ? Î?”]

Figure 12: Table entry

endprocedure

Figure 13: ?

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